A LOW POWER LOW VOLTAGE BIOMEDICAL SIGNAL ACQUISITION CHIP

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NATIONAL UNIVERSITY OF SINGAPORE

2008

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A THESIS SUBMITTED

FOR THE DEGREE OF MASTER OF ENGINEERING

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

NATIONAL UNIVERSITY OF SINGAPORE

2008

Acknowledgement

I am grateful to my supervisors Assoc. Prof. Xu Yong Ping, National University of Singapore for providing me with the valuable opportunity of conducting research under his supervision. I sincerely thank him for his guidance, support and help throughout the course.

I would like to thank Mr. Teo Seow Miang and Ms. Zheng Huan Qun, Signal Processing and VLSI design laboratory, National University of Singapore, for helping me with setting up environment to carry out simulations and testing.

Special thanks to the Mediatek Singapore Pte. Ltd. for supporting me with a graduate research scholarship.

I thank my friends in the Signal Processing and VLSI design laboratory, National University of Singapore, especially Mr. HeLin, Mr. Chen Jian Zhong and Mr. Yang Zhenglin, whose association making these two years an enjoyable research experience.

Finally, I thank my parents and my wife for their constant encouragement, understanding and blessings towards my endeavor.

Table of Contents

Summary

In recent years, numerous researches are done on non-invasive medical diagnostic as the method is suitable to provide essential information without invasive measures. One of the main focuses is on portable medical devices which emphasizes on real-time monitoring. Bio-signals of interest in recent researches include ECG (Electrocardiogram) and EEG (Electroencephalogram) signals.

To suit into long-term recording or monitoring, an ideal portable device would be highly integrated and fully portable. However such devices would have stringent requirements on supply voltage and power consumption.

On top of that, ECG signal is usually weak in magnitude (in terms of mV) and in the range of low frequencies (0.1 to 150 Hz), which means the signal could be easily masked by flicker noise. It is essential for the device to have ultra low input referred noise to pick up the ECG signal. In addition, large DC offset due to the electrochemical interface between electrode and human skin needs to be rejected during signal acquisition.

This work presents a low power low voltage ECG signal acquisition IC chip. The overall system consists of a low noise instrumentation amplifier (LN-AMP) with DC offset rejection, and an 11 bit successive approximation analog-to-digital converter (SA-ADC).

The LN-AMP is basically a pseudo-differential amplifier with differential input and single-ended output structure. Diode-connected PMOS transistors are used as pseudo-resistor, which have resistance in the order of $10^{12}\Omega$, to form an ultra-low cut-off frequency high pass filter with input capacitors to reject DC offset. The low noise OTA

(LN-OTA) is using a standard current mirror OTA design. The transistor sizes are optimized to achieve a low input referred noise OTA with reasonable phase margin and power consumption.

Successive approximation approach is used in the ADC design. This is due to SA-ADC attains a well balance between resolution, speed, and circuit complexity. The architecture of SA-ADC is modified from conventional structure so that the converter can achieve full swing input range. To conserve power consumption, several tactics are used in the design. The sample-and-hold (S/H) operation is integrated into the LN-AMP output stage and thus no additional power is needed for S/H operation. Meanwhile, MSB capacitor array is "split" into a sub-array which is identical to the rest capacitor array so that switching energy is reduced during conversion phase. In addition, comparator circuits are turn off during sampling phase and only active during ADC conversion phase. Finally, serial output design is employed to reduce digital circuit complexity and thus power consumption.

Overall system was implemented in AMS 0.35µm standard CMOS process and the design performance was verified by post-layout simulation. The fabricated chip was measured to extract the performance statistics. Overall integrated system is consuming 4µW under 1.5V supply voltage. The measured input referred noise is 1.862µV_{rms} while the bandwidth is 5mHz to 190Hz. Overall system achieves effective number of bit (ENOB) of 9.3 bit with 500S/s sampling rate.

In conclusion, there is still research window opened for improvement on the ECG signal acquisition chip. Future development to integrate with RF circuit for wireless transmission is a possible pathway.

List of Figures

List of Tables

List of Abbreviations and Symbols

ECG	Electrocardiogram
EEG	Electroencephalogram
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CMOS	Complementary MOSFET
NMOS	N-channel MOSFET
PMOS	P-channel MOSFET
IC	Integrated Circuits
L	Channel Length of the MOSFET in μm
W	Width of the MOSFET in μm
V_{th}	Threshold voltage of the MOSFET in V
μC_{OX}	mobility constant
g_m	transconductance
t_{ox}	Gate oxide thickness of the MOSFET in nm
DC	Direct Current
AC	Alternating Current
BSIM	Berkeley Short-channel IGFET Model
EKV	Enz-Krummenacher-Vittoz MOS model
DUT	Device under test
OTA	Operational transconductance amplifier
LN-AMP	Low noise amplifier
LN-OTA	Low noise operational transconductance amplifier

ADC	Analog-to-digital converter
DAC	Digital-to-analog converter
SAR	Successive approximation register
S/H	Sampling-and-hold
A/D	Analog-to-digital
MSB	Most significant bit
LSB	Least significant bit
DNL	Differential non-linearity
INL	Integral non-linearity
SNR	Signal-to-noise ratio
SQNR	Signal-to-quantization-noise ratio
SINAD	Signal-to-noise-and-distortion ratio
ENOB	Effective number of bit
THD	Total harmonic distortion
CMRR	Common mode rejection ratio
PSRR	Power supply rejection ratio

CHAPTER 1 Introduction

Non-invasive diagnostic technology is a wide field incorporating techniques such as X-ray, tomography, MRI and ultrasound in purpose of gaining knowledge on the functioning of human body during treatment of a patient. Since bio-signals are acquired from body surface, the non-invasive methods are ideally suited to provide essential data to clinician for analysis and treatment. These bio-signals are translated into useful electric signals through acquisition devices and ideally suited for post-processing, displays and storage.

1.1 Overview

Following rapid advancement in biomedical engineering in recent years, numerous researches are done in exploring fast and accurate diagnostic instrumentation. One of the main focuses in non-invasive medical diagnostic is on portable medical instruments. The portability of medical instruments gives more freedom of movement to patients without restricting patients' mobility, which is in particular important in long duration examination and real-time monitoring.

The development of VLSI techniques in realizing biomedical devices enables miniaturization and portability of such diagnostic systems. Successful monitoring of patients' diagnostic signals using portable devices, had been performed on out-fields physiological studies [1-2][6-8].

Among bio-signals of interest, heart activity is one of the popular bio-signals targeted by research activities in designing the acquisition system. Electrocardiogram (ECG) records the electrical signal produced by the heart activity over time and has been

widely used for investigation and diagnostic of heart diseases. The electrical signal can be measured at selectively placed electrodes on the skin where the ECG displays the voltage between pairs of these electrodes. This display indicates the overall rhythm of the heart, and weaknesses in different parts of the heart muscle. It is the best way to measure and diagnose abnormal rhythms of the heart [3] particularly abnormal rhythms caused by damage to the conductive tissue that carries electrical signals, or abnormal rhythms caused by levels of dissolved salts [4]. A typical ECG signal is shown in Figure 1.1.

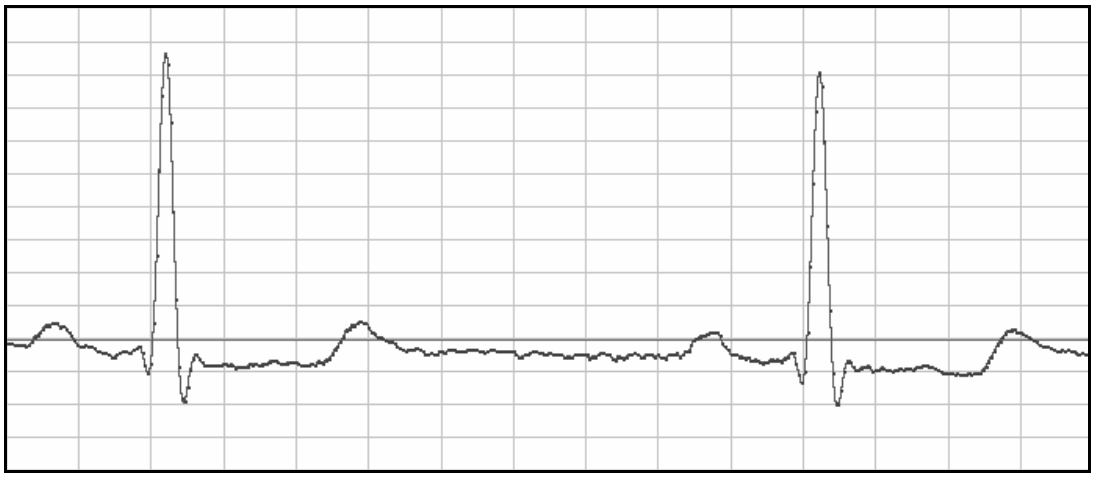


Figure 1.1 A typical ECG signal graph.

1.2 Motivation

The motivation behind this work is to explore the design of a low power low voltage ECG signal acquisition IC chip. In the use of portable medical devices, the ultimate goal is to make the patient of study unconscious of the existence of the recording devices while long term monitoring process is taking place. To suit into long-term recording or monitoring, an ideal portable medical device would be highly integrated and fully portable.

However such devices would have stringent requirements on supply voltage and power consumption. To achieve full portability, button cell battery is always the choice for such portable medical devices. This requires the devices to operate under very low supply voltage and ultra low power consumption to enhance the recording length and duration.

In addition, such system is usually used in a noisy environment. ECG signal is usually weak in magnitude (up to 5mV) and in the range of low frequencies (0.1 to 150 Hz) [5][8], which means the signal could be easily masked by flicked noise. It is essential for the device to have ultra low input referred noise (maximum $10\mu V_{rms}$ in-band input referred noise) to pick up the ECG signal [8]. Apart from that, large DC offset is produced due to the electrochemical interface between electrode and human skin during signal acquisition. The DC offset can be as large as ±300mV [5][8] and saturate the output of the device. Thus the device needs to have very good DC offset rejection.

1.3 Scope of this work

This work presents the research works in designing a low power low voltage ECG signal acquisition IC chip. The overall integrated system architecture consists of an input Low Noise Instrumentation Amplifier (LN-AMP) with DC offset rejection function, and an 11 bit Successive Approximation Analog-to-Digital Converter (SA-ADC). Optimization of device sizes was carried out to achieve low input referred noise of overall. Careful trade-off was considered in current consumption, stability and linearity during improvement on noise performance. Different methods to conserve power consumption were explored and incorporated in the design of LN-AMP and SA-ADC. Finally the design was implemented using AMS 0.35µm standard CMOS process technology. Different test setups and measurements were performed on the fabricated chip to extract the performance of the design.

1.4 Organization of thesis

Chapter 1 gives an overview on the bio-signal acquisition chip and motivation of low power low voltage design. This chapter covers the scope of this work and the organization of the thesis as well. Chapter 2 focused on review of past works in bio-signal acquisition chip design. A summary on amplifier noise and overview on prior arts in low noise low power amplifiers are presented. A brief elaboration of ADC types and previous works on low power low voltage ADCs are illustrated as well. It is shown that the SA-ADC achieves a great balance between conversion speeds, resolution and circuit complexity among different choices of ADCs.

In chapter 3, details on the design of this ECG signal acquisition chip are discussed. Overall chip architecture and operation is described in this chapter. The design of LN-AMP, including the optimization of the low voltage low noise OTA is explained. Careful considerations were taken in achieving a well-balanced trade-off between input referred noise, power consumption, output voltage swing and stability. Following that, the design of the low voltage low power SA-ADC and individual blocks in the ADC are presented in details. Different tactics in lowering the power consumption were engaged in the chip design.

Chapter 4 illustrates overall system implementation and verification. The design was implemented in AMS 0.35µm standard CMOS process technology. Careful layout consideration was taken in the layout design to avoid jeopardizing the performance of the chip. Post-layout simulations were performed to verify the performance of the chip.

Following the fabrication of the design, chapter 5 presents the measurement results of the chip. Test setups to extract the statistics of the chip are described. Detail discussions on the measurement results are illustrated in this chapter also. Finally chapter 6 depicts the conclusion of this work. Suggestions for future enhancements of this work are presented in chapter 6.

CHAPTER 2 Review of Previous Work

This chapter gives a brief review of prior art of the states on low power low voltage bio-signal acquisition chip. As mentioned in chapter 1, overall integrated system in this signal acquisition chip includes a Low Noise Amplifier (LN-AMP) and a Successive Approximation Analog-to-Digital Converter (SA-ADC). Amplifier noise is analyzed in the first section and low noise low power Instrumentation Amplifier (IA) designs are reviewed following that. Different ADC architectures are briefly discussed and prior works in low power low voltage ADCs are investigated in the latter portion.

2.1 Low Noise Low Power Amplifiers

To acquire the weak input ECG signal, the acquisition chip needs to have an ultra-low input referred noise. From the view of system, the system input stage determines the overall system input referred noise and sensitivity. This can be described by Friis Formula shown in equation (2.1) [9].

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots \tag{2.1}$$

F is the noise factor of overall system, F_1, F_2 and F_3 are the noise factor of the first block, second block and third block of a system, while $G_1$and G_2 are the gain of the blocks respectively. Noise factor is given by the ratio of input Signal-to-Noise Ratio (SNR) to output SNR, where this ratio would give estimation on the noise effect from a particular stage in the system. Smaller noise factor indicates lower noise effect from an individual block.

From equation (2.1), it can be seen that as long as the amplification of the front input stage is large enough, the later stages in a system has limited effect on overall system input referred noise. Hence the noise performance of the input stage of the system is particularly important and this the main purpose of designing a low noise input amplifier.

2.1.1 Noise Sources in CMOS Amplifiers

There are two main noise sources named inherent noise and interference noise [10]. Interference noise is unwanted intervention from external world on the circuit. Meanwhile, inherent noise refers to noise induced by the devices in the circuit due to their fundamental properties. Inherent noise can be reduced through proper circuit design and hence low noise amplifier design deals with reducing inherent noise.

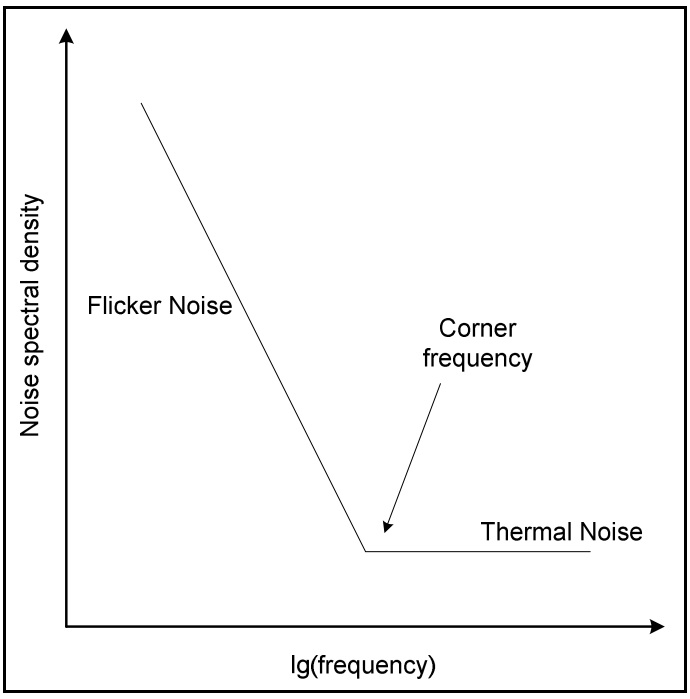


Figure 2.1 A typical CMOS amplifier noise spectrum.

A typical noise spectrum of CMOS amplifiers is shown in Figure 2.1. From the figure, it can be seen that the input referred noise is dominated by a flat noise spectrum at high frequencies. This part of the noise curve is termed as thermal noise floor where the dominant noise source is named thermal noise or white noise [10][17].

At lower frequencies, the dominant noise source is flicker noise. Unlike the constant thermal noise floor, flicker noise is inversely proportional to frequency. Detail description on flicker noise can be referred to [11]. While thermal noise and flicker noise are the main noise sources of CMOS amplifiers, the frequency at which flicker noise is equal to thermal noise, is named corner frequency.

As the ECG signal lies in the low frequency range (0.1 to 150Hz), it appears that the flicker noise is the main noise source. It is essential to minimize the flicker noise of the low noise amplifier while keeping the corner frequency as low as possible to reduce the flicker noise component. In addition, it is necessary to keep a low white noise level as well to avoid the thermal noise becoming the dominant noise source instead.

2.1.2 Low Noise Low Power Amplifier Design

Several low noise low power amplifier design for ECG signal acquisition chip had been reported in previous works. Various techniques had been used in these works to achieve both low noise and low power requirements.

In [8], a differential difference amplifier (DDA)-based non-inverting Instrumentation Amplifier (IA) is used as the input stage amplifier of an EEG/ECG analog front-end IC. The architecture of the DDA-based IA is shown in Figure 2.2.

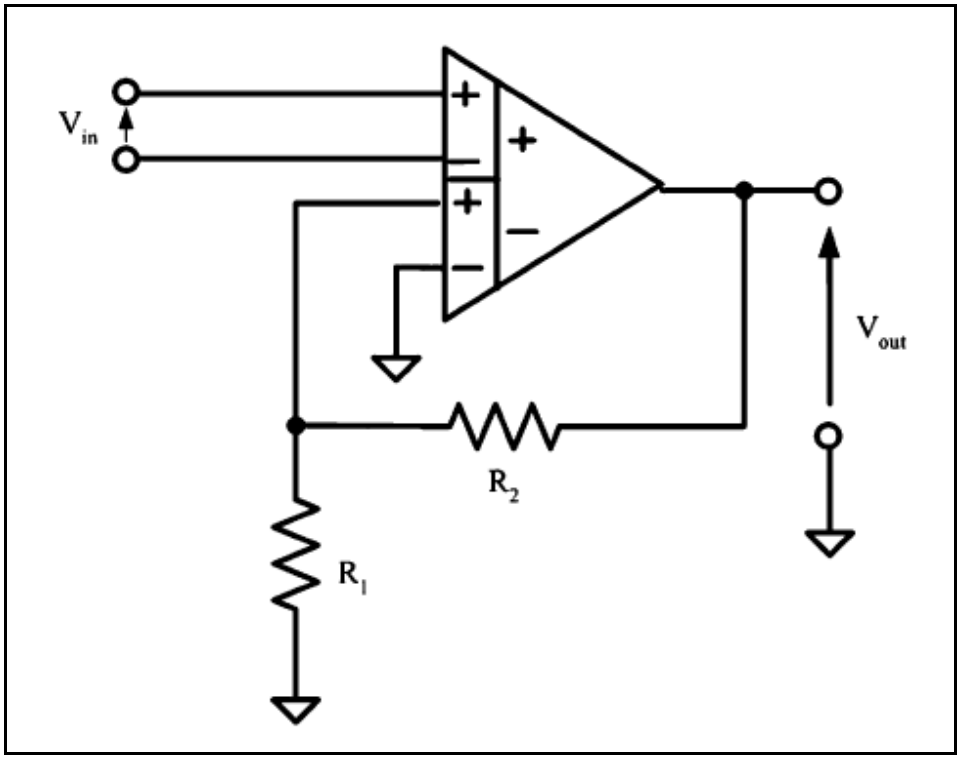


Figure 2.2 A DDA-based IA architecture.

From Figure 2.2, the Common Mode Rejection Ratio (CMRR) of the DDA-based IA is affected by the input ports while the mismatch between resistors R_1 and R_2 affects the gain factor. Hence, chopper stabilization technique is incorporated in this amplifier. The chopper stabilization would allow higher tolerance to input port mismatch, thus achieving high CMRR with low input offset and low flicker noise at the same time. However, incorporating a chopper circuit would require additional clock and control circuit which adds to extra power consumption.

Apart from that, the architecture in [8] requires a rail-to-rail input IA due to the high DC offset characteristic of ECG signals. This adds to more stringent challenges in the

amplifier design where additional input transistors maybe needed, causing higher input referred noise and higher current consumption.

To tackle the high DC offset issue, a low noise low power amplifier design is shown in [12]. The architecture is shown in Figure 2.3. It is a capacitor-based feedback amplifier with the use of pseudo-resistors in the feedback network.

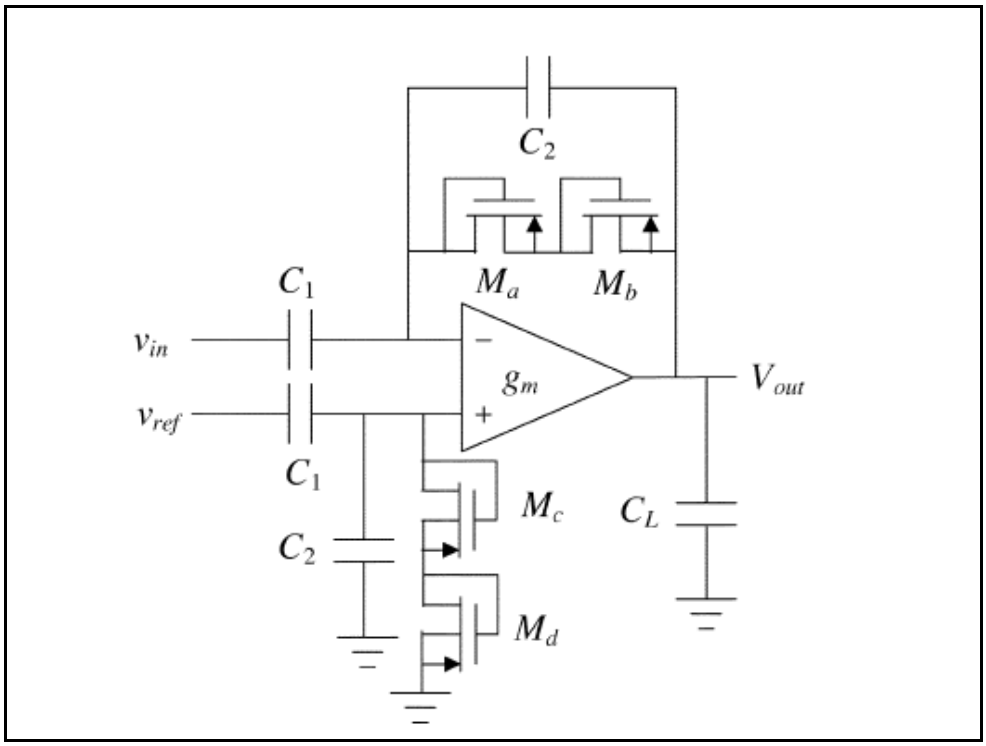


Figure 2.3 Low noise amplifier architecture in [12].

The use of diode connected PMOS transistors as pseudo-resistors has relaxed the requirement on DC offset rejection design. Compared to [8], there is no need to include the chopper stabilization circuit which adds to power consumption. Apart from that, the current consumption is used efficiently in [12] to achieve an optimized LN-AMP.

However, the LN-AMP in [12] operates under a high supply voltage of 5V. For portable device application, battery cells are usually used as the power supply. As the battery cell usually has a supply voltage of 1.5V, this makes the design unsuitable for portable medical instruments. If the design is to be used in low voltage application, more efforts need to be done to resize the transistors.

Another improved LN-AMP is presented in [13] with dedicated specifications for ECG signal application.

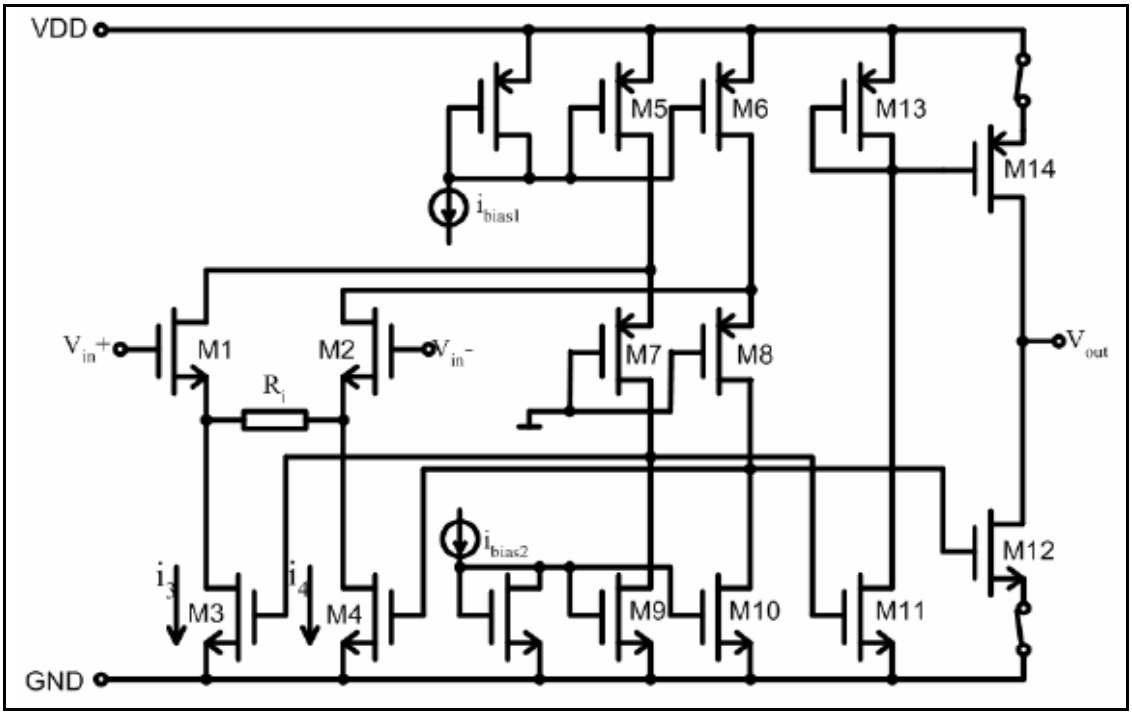


Figure 2.4 Low noise OTA used in [13].

In [13], the LN-AMP is using the exact architecture in [12] while the bandwidth is set to 245Hz. The LN-OTA proposed used an internal feedback in the OTA, as shown in

Figure 2.4. This would achieve a higher input transconductance and hence attaining lower input referred noise.

However, the output stage has little limitation on dynamic current consumption though the DC current consumption is set to 330nA. Since the architecture is dynamic in nature with switches incorporated in the output stage, the overall power consumption may still be high. Besides that, the input referred noise reported is still as high as $2.7\mu V_{rms}$. Since an 11 bit ADC with 1V supply voltage is used in [13], a LSB when reflected at system input is only $4.9\mu V$.

Considering the issues discussed above, the input referred noise in this design is set to be lower with reference to these architectures. Further discussion on the design of LN-AMP in this research work will be presented in Chapter 3.

2.2 Low Power ADCs

In most of the systems nowadays, post-processing in digital domain is unavoidable since this would be more power efficient and easier to implement than an analog circuit. Hence an ADC is almost a necessity in all integrated system. In ECG signal acquisition chip, ADC serves the same function and has the same important role.

Since the acquired bio-signal is meant for displays, records and storage, the analog-signal must be converted into digital signal. As mentioned in chapter 1, the main requirement on the ADC in such medical device is on the power consumption. Several ADC architectures will be reviewed subsequently and followed by prior works in low power ADC design.

2.2.1 ADC Architectures

There are various ADC architectures available while not all of them suitable for low power low voltage application. Several of the main ADC architectures are discussed here, which includes flash (parallel), two-step (sub-ranging), integrating (serial), and successive approximation. Each type has each own advantages and a brief description on these architectures will be elaborated in the following.

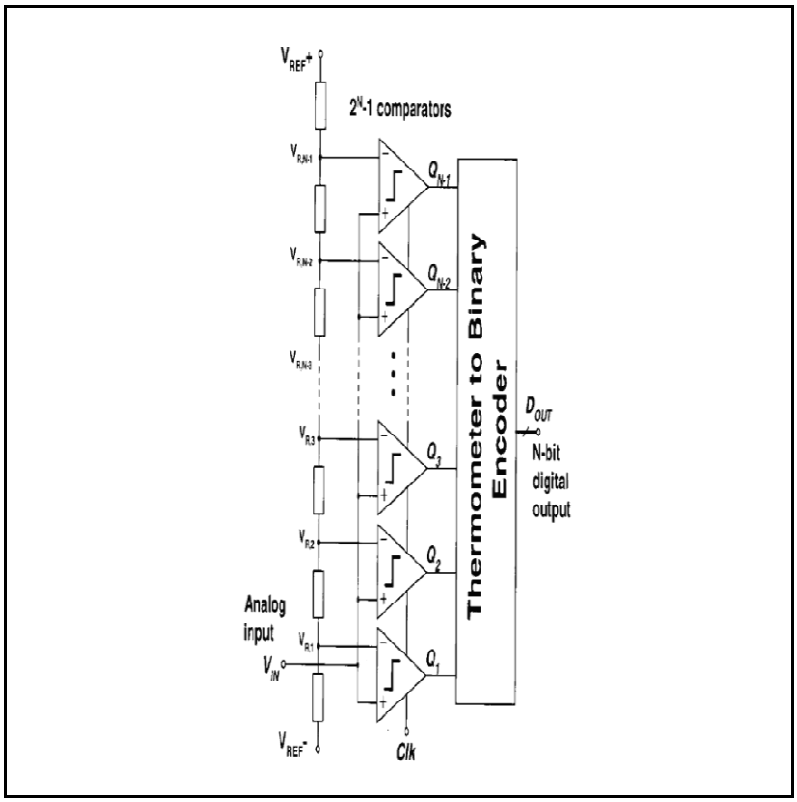


Figure 2.5 General flash ADC architecture.

A general architecture of flash ADC type is shown in Figure 2.5. Flash ADC is the fastest ADC and has the simplest architectures [14]. In Figure 2.5, the flash ADC performs 2^N level quantization with (2^N-1) comparators. A resistor ladder is usually used

to generate the reference voltage level. Since the input signal is directly connected to comparator inputs, flash ADC has very fast speed with the only limitation from comparator speed. However, the drawback of flash ADC is that the number of comparators needed grows exponentially with number of bits. The area needed and power consumption is so large that it is not practical for portable application.

Another type of ADC is a two-step converter, also named as sub-ranging ADC. The architecture is shown in Figure 2.6.

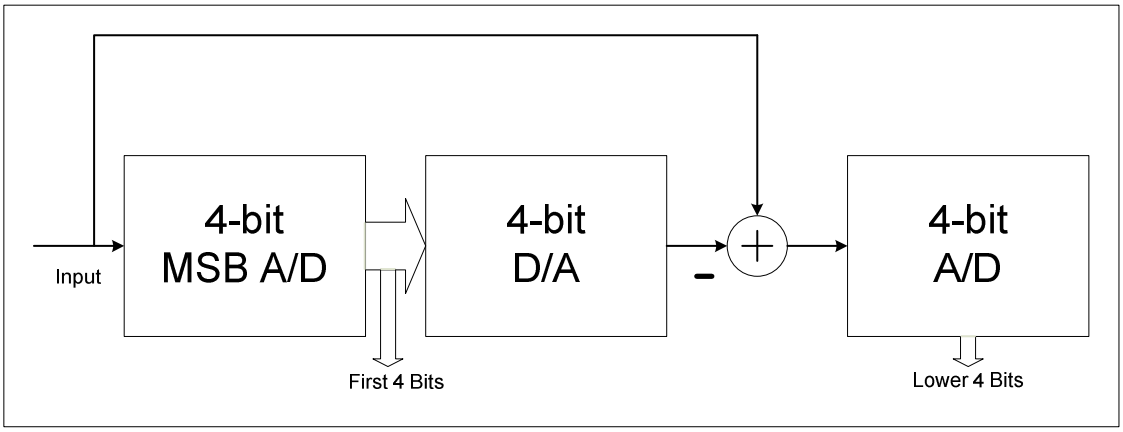


Figure 2.6 A general 8 bit two-step ADC architecture.

In spite of a slower speed, the two-step converter consumes less silicon area and dissipates less power than the flash ADCs [10]. Using an 8-bit ADC as example, the 8-bit flash ADC requires 256 comparators while the two-step ADC needs only 32 comparators. Although at least two clock cycles needed for each conversion, the throughput still approaches that of flash converters.

Nevertheless, the two-step converter is not a best choice as the circuitries needed still considered excessive leading to undesired power dissipation. In addition, high conversion speed is not utmost important in a bio-signal processing system.

Following this, a dual slope integrating ADC is shown in Figure 2.7. Integrating ADC is a serial type converter and is a popular choice in high accuracy application with slow signals [10]. The main advantages of integrating ADC are very low offset and gain errors, highly linear, and very high resolutions.

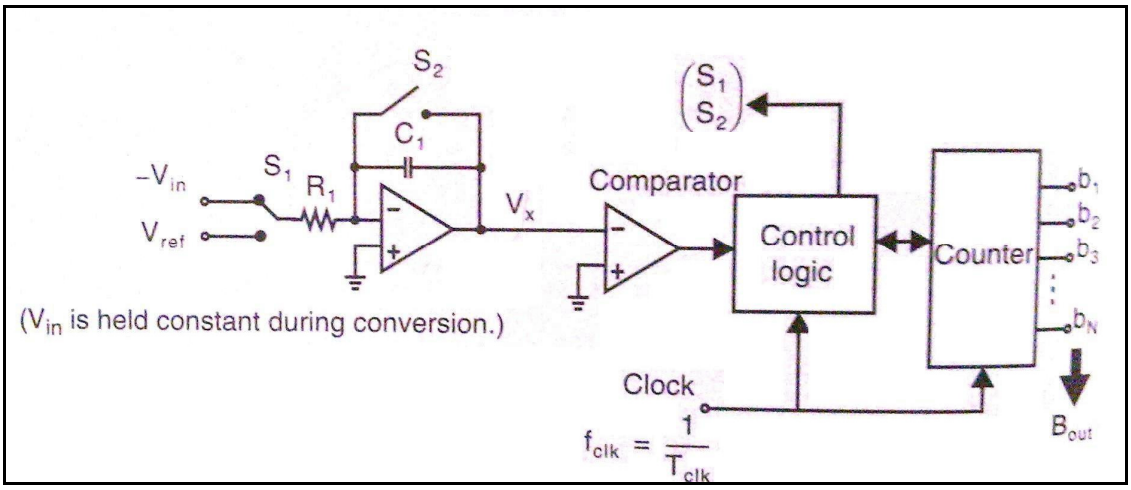


Figure 2.7 A general dual-slope integrating ADC architecture.

The main drawback of integrating ADC is the very slow speed in conversion. In an N-bit converter, a worst case of 2^{N+1} clocks is needed for conversion. For ECG signal with a bandwidth of 150Hz, the Nyquist sampling rate would be at least 300Hz to avoid aliasing. Under this circumstance, an 11-bit integrating converter would need a 1.23MHz clock frequency. Such a high speed clock rate would rather increase the power

consumption of the overall system. Hence the integrating ADC may not be an ideal choice for ECG signal acquisition chip.

As for the Successive Approximation A/D converter (SA-ADC), it is one of the most popular approaches due to reasonable conversion speed yet moderate circuit complexity [10]. A D/A converter based SA-ADC architecture is shown Figure 2.8. Due to the mentioned advantages, the SA-ADC is the main choice in low power system such as a bio-signal acquisition chip. The operation of SA-ADC is to be further discussed in Chapter 3.

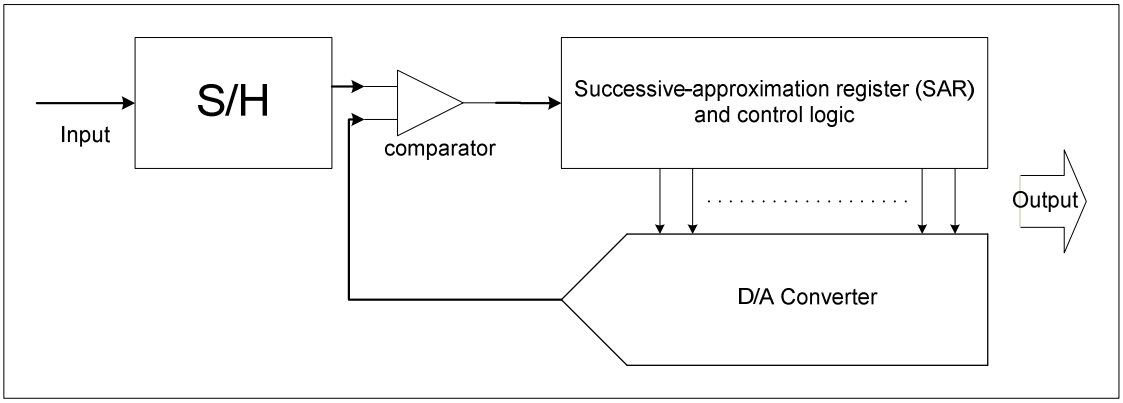


Figure 2.8 D/A converter-based SA-ADC architecture.

2.2.2 Low Power ADC Design

In portable medical devices, low power and operation under low supply voltage are the main design challenges. Successive approximation ADC (SA-ADC) achieves a well-balanced performance in different aspects. Hence in most bio-application chip, SA-ADC architecture is chosen. Several low power low voltage ADC designs had been reported [13], [15] and [16] with all of them using SA-ADC architecture.

A SA-ADC reported in [15] is able to operate under a supply voltage as low as 0.5V with a modified architecture from ordinary structure, as shown in Figure 2.9.

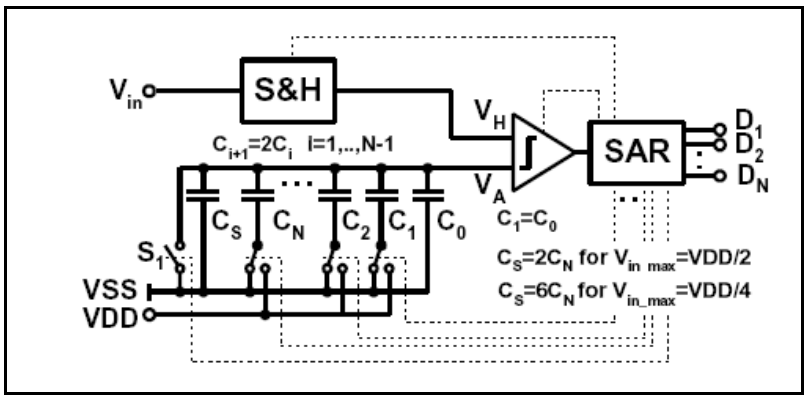


Figure 2.9 A modified low voltage SA-ADC architecture in [15].

The main modification is that the DAC capacitor array is separated from the input node, making operation under an extremely low supply voltage possible. However, while the ADC resolution is only up to 9-bit with 1V supply voltage, this architecture cannot achieve rail-to-rail input range due to limitation on the comparator input common mode range at the capacitor array side.

In addition, an extra holding capacitor is needed at the ADC input to hold the input throughout the conversion phase. An external capacitor is used where this is not preferred for portable device design. Since the sampling rate for ECG signal acquisition chip is rather low, using integrated on-chip holding capacitor instead consumes excessive area making fully integrated system impossible.

Another modified SA-ADC reported in [16] operates under 1V supply voltage and is able to achieve rail-to-rail input range. The architecture is shown in Figure 2.10.

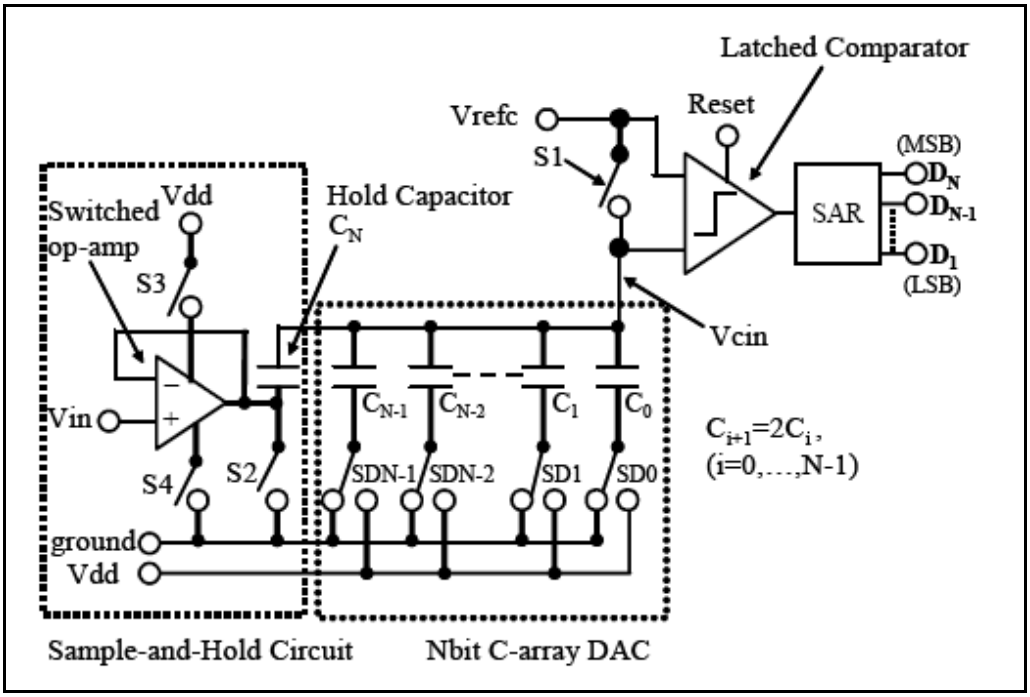


Figure 2.10 A modified low voltage SA-ADC architecture in [16].

The capacitor C_N, which also acts as a holding capacitor, is used to scale down the input voltage V_{in} to V_{cin}. This makes a rail-to-rail input range possible under a low supply voltage operation. However, the scaling capacitor C_N is still very large so that the voltage can be scaled down sufficiently. In [16], a small unit capacitor of 50fF is used to avoid very large C_N. This may not be sufficient to meet the matching requirement for 11-bit accuracy.

To tackle both issues of input voltage range and area usage, a modified architecture for SA-ADC was proposed in [13], as shown in Figure 2.11.

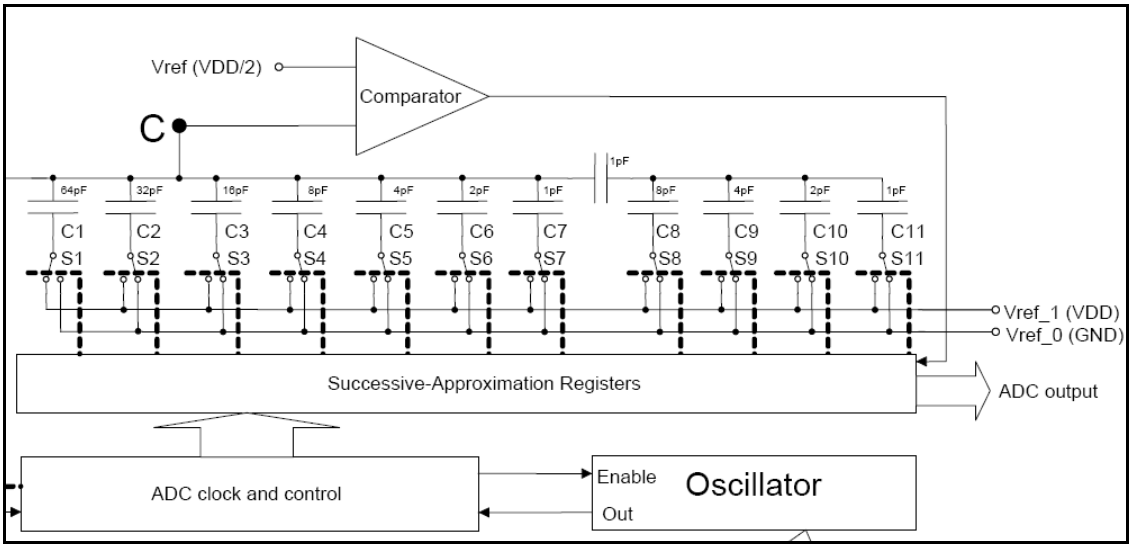


Figure 2.11 A modified low voltage SA-ADC architecture in [13].

In the architecture of [13], a rail-to-rail input range is achieved as long as the reference voltage of the comparator encompasses $V_{DD}/2$. Since the DAC capacitor array is used as holding capacitor, there is no additional area needed in the integrated chip. However, a 1MHz clock frequency is used in [13] causing a higher power consumption in the converter. The SA-ADC consumes more than 80% of the total 2.3µA current consumption. Hence an improvement on the converter power efficiency is needed.

The proposed ADC in this research work would be using the SA-ADC architecture with reference to [13]. Detail discussions to tackle on the power consumption issue will be presented in Chapter 3.

2.3 Summary

In this chapter the basics of LN-AMP and ADC are discussed. The need of a low noise instrumentation amplifier was illustrated and the noise sources in an amplifier were introduced. Following that, several prior works in LN-AMP were presented where the advantages and short-comings were discussed in details. The proposed LN-AMP design in this research work used a capacitive feedback amplifier with pseudo-resistor as this architecture presents a very good DC offset rejection performance.

In the later portion, different types of A/D converters were briefly explained and analyzed on the advantages and disadvantages. Due to a well-balanced trade-off between speed, resolution and circuit complexity, the SA-ADC architecture was chosen for the ADC design in this chip. Several low voltage low power SA-ADC designs were analyzed. The proposed SA-ADC in this integrated chip used a rail-to-rail input architecture with improvement on power consumption over the prior designs.

CHAPTER 3 Acquisition Chip Design

This chapter describes the design of the low power low voltage ECG signal acquisition chip in this research work. The overall chip architecture is presented in the first part of the chapter. Following that, details on the individual blocks and design considerations will be further elaborated. Specifications and device dimensions are summarized in the latter part of the chapter.

3.1 Overall Chip Architecture

The overall ECG signal acquisition chip includes a Low Noise Amplifier (LN-AMP) and a Successive Approximation Analog-to-Digital Converter (SA-ADC). The overall block diagrams are shown in Figure 3.1.

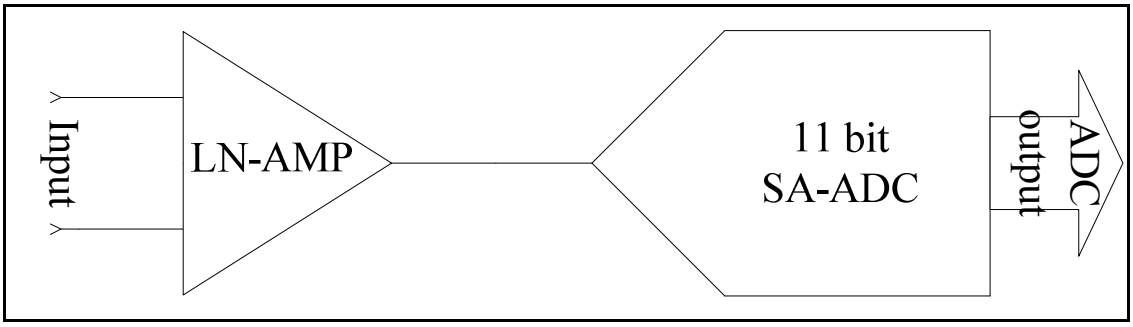


Figure 3.1 Overall design architecture.

The basic considerations in designing the system architecture are illustrated in the following. Since the ECG signal is analog in nature, an analog input block is needed to acquire and amplify the signal. The ECG signal is generally weak and maximum magnitude is only up to 5mV as mentioned in Chapter 1 [5][8]. Considering this, the overall system needs to have ultra low input referred noise. As described in Friss formula given by equation (2.1), input stage would decide the overall input referred noise. Hence the input LN-AMP is essential.

As mentioned in Chapter 2, data processing and storage are mainly done in digital domain in modern systems, which make analog-to-digital conversion inevitable. Following the LN-AMP is an 11 bit SA-ADC to convert the acquired analog data into digital output for post-processing. Other analog processing is incorporated into the LN-AMP or is shifted into digital domain to further conserve the power consumption. For example, the 50Hz analog notch filter is not integrated in the system as it will be more power-efficient to implement a digital notch filter.

The detail designs of the individual blocks are elaborated in the later sections.

3.2 The Design of Low Noise Amplifier

The considerations in deciding the specifications of the LN-AMP are discussed in this section. In setting the specifications of the LN-AMP, among the main considerations are the amplifier gain, bandwidth, stability, input referred noise and power consumption. The voltage gain of the LN-AMP is set to 200V/V, which is equivalent to 46dB. This would amplify the maximum ECG signal magnitude of $5mV_{PP}$ to $1V_{PP}$ at LN-AMP

output. Considering the ECG signal bandwidth of 0.1Hz to 150Hz, the 3dB high pass cut-off frequency is set to 0.1Hz.

As for the 3dB low pass cut-off frequency, the specification has to meet at least 150Hz while not too high due to two reasons. Firstly from noise consideration, higher bandwidth would induce higher in-band input referred noise. Even if the noise floor at higher frequency can be kept lower so that in-band integrated noise is reduced, this is usually done at the expense of power consumption.

Secondly higher bandwidth usually costs more power consumption as more current is needed at the output stage to drive the same load. In addition, designing a lower bandwidth would keep the amplifier functioning as an anti-aliasing filter at the same time. Hence the filter function is integrated in the LN-AMP to save the power consumption of realizing an additional filter.

As for the input referred noise, the specification is desired to be as low as possible with reference to prior works discussed in Chapter 2. With referenced to [8], the input referred noise has to be lower than $10\mu V_{rms}$. Meanwhile considering that an 11-bit ADC with 1.5V supply voltage is designed, one LSB reflected at the LN-AMP input would be $3.7\mu V_{rms}$, even lower than the desired specification. Hence the input referred noise is targeted to be $1.5\mu V_{rms}$ or below, which will be less than half LSB. However, a balance trade-off has to be considered in the design process due to more current is needed to keep the noise level low.

The design specifications of the LN-AMP are summarized in Table 3.1.

Parameter	Value
Gain	200V/V
Bandwidth	<0.1Hz to >150Hz
Input referred noise (in-band)	$<1.5\mu V_{rms}$
Supply voltage	1.5V
Current consumption	As low as possible

Table 3.1 LN-AMP Specifications Summary.

3.2.1 Low Noise Amplifier Design

The architecture of the LN-AMP is shown in Figure 3.2. The LN-AMP is using pseudo-differential amplifier structure with differential input and single-ended output design. The input of LN-AMP is connected to input capacitors C_1 while the output is feedback from the Low Noise Operational Transconductance Amplifier (LN-OTA) output to the LN-OTA input through feedback capacitor C_2. An OTA is used in the amplifier due to the amplifier output is driving a capacitor load, C_{DAC} which is the digital-to-analog converter (DAC) capacitor array of the SA-ADC. C_{DAC} has a value of approximately 128pF and also acts as the holding capacitor for sample-and-hold (S/H) operation.

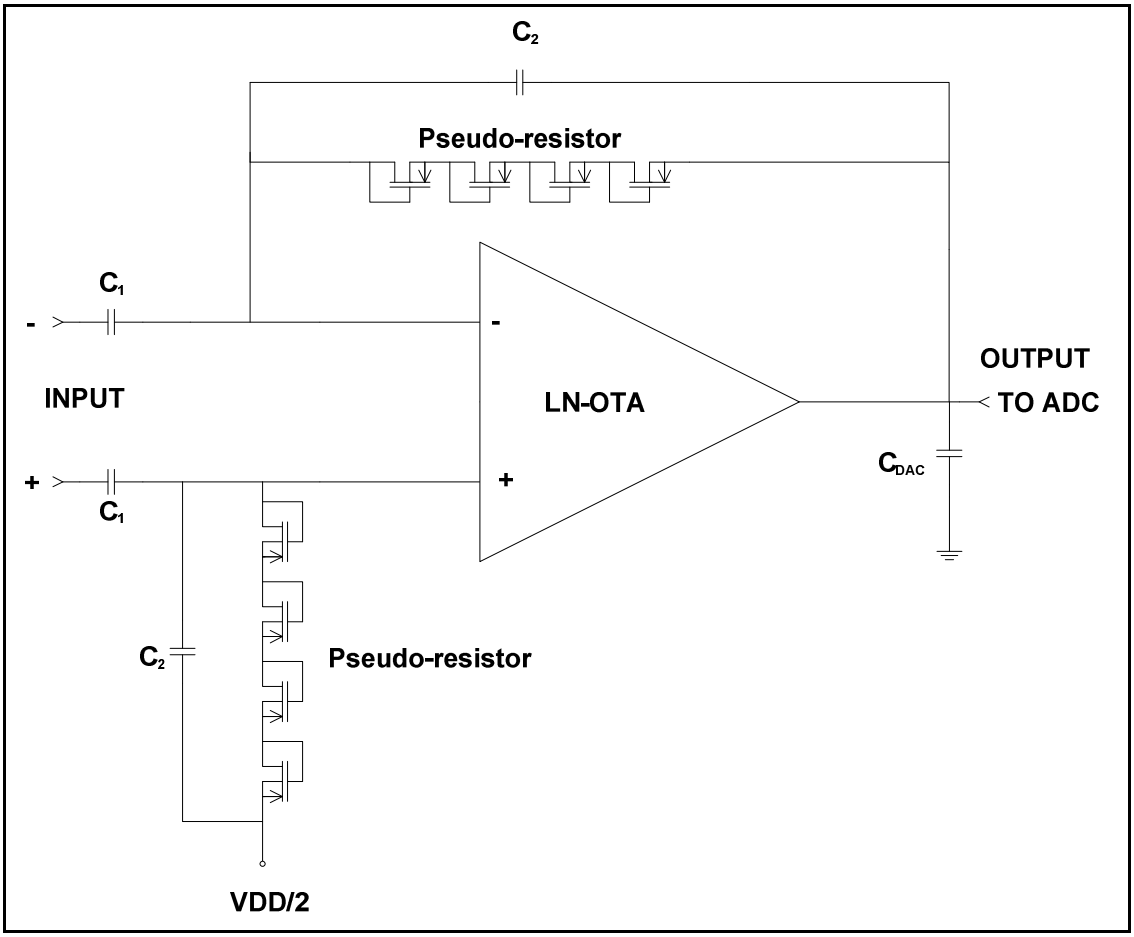


Figure 3.2 Low noise amplifier (LN-AMP).

The amplifier mid-band gain, A_m is set by the ratio of C_1/C_2. To meet the gain specification, the ratio of C_1/C_2 is set to be 200, which is equivalent to 46dB. In deciding the capacitor value, factors to be considered are capacitor area and device matching. Lower capacitance has a smaller area in layout but larger mismatch between devices. Mismatch between C_1 and C_2 leads to deviation from the designed gain.

However, there is a limit to the implementation of an on-chip capacitor. The capacitor size has to be reasonable to realize a fully integrated system. The value of C_2 is

chosen to be 0.3pF while C_1 is set to 60pF to achieve balance trade-off between area utilization and device matching.

The 3dB low pass cut-off frequency is approximately set by $g_m/ (A_mC_{DAC})$ where g_m is the transconductance of LN-OTA. This is assumed that the value of C_{DAC} is larger than C_1 and C_2. Given that C_{DAC} is designed to be 128pF and C_1 is set to 60pF, the assumption would be valid in this design.

As mentioned in Chapter 1, the ECG signal has a large DC offset components due to electrochemical reaction between interface of electrodes and human skin. This DC offset input can be as high as ±300mV and may saturate the amplifier output. Thus the embedded DC offset in the ECG signal needs to be rejected.

To achieve a good DC offset rejection, capacitor C_1 is used as the input in this design to block all DC components. At the same time, pseudo-resistors are used in this design to form a high pass filter with capacitor C_2. This high pass filter will decide the 3dB high pass cut-off frequency, which is given by $1/R_{pseudo}C_2$ where R_{pseudo} is the resistance of the pseudo-resistor.

Since the ECG signal bandwidth can be as low as 0.1Hz, time constant value of the high pass filter, $R_{pseudo}C_2$ has to be lower than 1.59. There is a limit to the capacitor size if the system is to achieve full integration for portable device. Hence R_{pseudo} has to be extremely large to achieve the desired bandwidth. A diode-connected PMOS transistor would act as the pseudo-resistor to provide the needed resistance.

As shown in Figure 3.2, each diode-connected PMOS transistor is a MOS-bipolar device which functions as a pseudo-resistor that provides the DC feedback cum DC biasing paths. When biased with negative V_{GS}, the device is a diode-connected PMOS

transistor. If biased positively with V_{GS}, the parasitic diode-connected source-well-drain p-n-p bipolar junction transistor (BJT) is activated [23].

According to [12], MOS-bipolar transistors are able to achieve resistance of more than $10^{11}\Omega$ for amplitude of 0.2V with a 4µm x 4µm sized transistor. This is as shown in Figure 3.3.

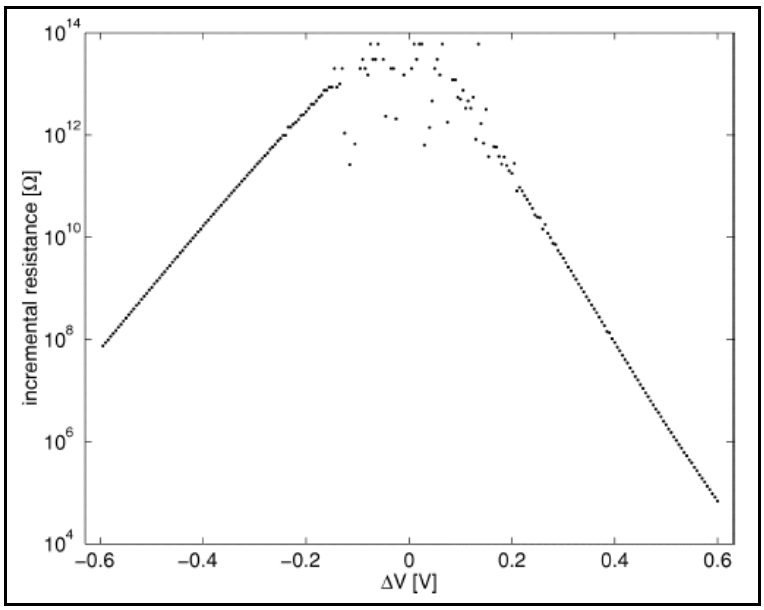


Figure 3.3 Incremental resistance of single MOS-bipolar element [12].

Despite the high incremental resistance, four MOS-bipolar devices in series were used in this design to achieve a very low 3dB high pass cut-off frequency, ω_L. In overall, ω_L is given by $1/ (4r_{inc}C_2)$ where r_{inc} is the incremental resistance of a single MOS-bipolar device. The large time constant of $4r_{inc}C_2$ indicates the long settling time needed by the amplifier. However, due to the incremental nature, a large change at the input causes a large voltage swing over the devices, and hence reducing the pseudo-resistance.

This would help in improving the amplifier settling time. Apart from that, another advantage of additional MOS-bipolar devices in series is in reducing distortion for large voltage swing at the amplifier output [12].

The sizes of the devices in the LN- AMP are shown in table 3.2. The MOS device dimensions in LN-OTA will be presented in the latter section.

Device	Value
C_1	60pF
C_2	0.3pF
Pseudo-resistors, W/L (all identical size)	1µm / 4µm

Table 3.2 Device sizes of LN-AMP.

3.2.2 Low Noise OTA Design

The OTA used is in this design is a current-mirror OTA [10]. This is a standard circuit topology used for driving capacitive load. However, since it is used in a LN-AMP at the system input stage, input referred noise of the OTA is of main concern. Besides that, low supply voltage and low power consumption are the other two main considerations in designing the OTA. Hence, the sizing of the transistors is critical in the design. The circuit architecture of the LN-OTA is shown in Figure 3.4.

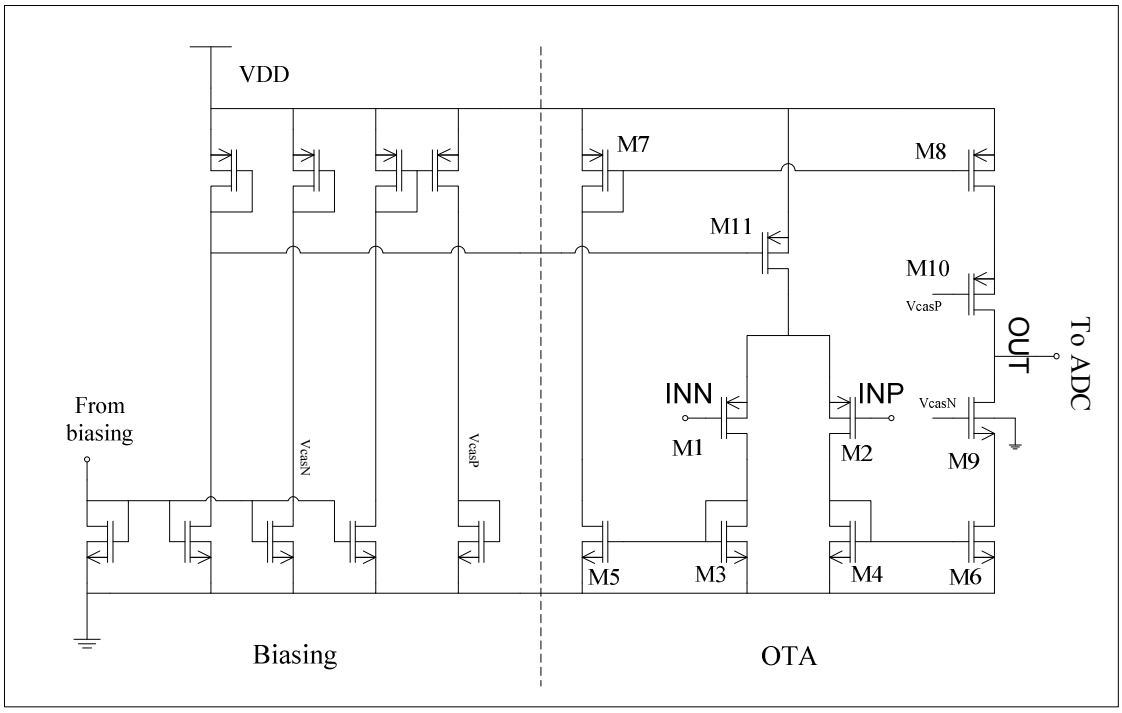


Figure 3.4 The schematic of LN-OTA circuit.

From noise analysis, the input transistors M_1-M_2 and the current mirror transistors M_3-M_7 are the main noise source contribution. Since the circuit is symmetrical, the approximate equivalent input referred noise is as depicted in equation (3.1).

$$\overline{v_{ni}^2} = 2\overline{v_{ni,1}^2} + 2\overline{v_{ni,3}^2} \cdot \frac{g_{m3}^{\ 2}}{g_{m1}^{\ 2}} + 2\overline{v_{ni,5}^2} \cdot \frac{g_{m3}^{\ 2}}{g_{m1}^{\ 2}} + 2\overline{v_{ni,7}^2} \cdot \frac{g_{m7}^{\ 2}}{g_{m1}^{\ 2}} \qquad (3.1)$$

$\overline{v_{ni,1}^2}$, $\overline{v_{ni,3}^2}$, $\overline{v_{ni,5}^2}$ and $\overline{v_{ni,7}^2}$ are the MOS device noise of transistor M_1, M_3, M_5 and M_7 looking at the gate respectively. It can be seen that the input transistors M_1 and M_2 are the main noise sources of the OTA.

As discussed in Chapter 2, there are mainly two types of noise in MOS device, which are the flicker noise and thermal noise. Since flicker noise is the dominant noise source in

low frequency range, the noise optimization starts from the flicker noise. The flicker noise of a MOS device looking at the gate is given by

$$\overline{v_{g,MOS}^2(f)} = \frac{K}{WLC_{OX}f} \tag{3.2}$$

where K is a constant depending on device characteristics and varies for different devices in the same process. W, L and C_{OX} represent the MOSFET's width, length and capacitance per unit area [17].

Since equation (3.1) reveals that the input transistors are the main noise contributor, PMOS transistors are used as the input transistors due to PMOS has a lower value of constant K. PMOS typically has a flicker noise magnitude of one to two order lower than NMOS as long as V_{GS} does not greatly exceed the threshold voltage [12][18][19].

Using transistors with larger gate size for M_1, M_3, M_5 and M_7 also reduces the flicker noise as shown in equation (3.2). However, in practice the transistors size cannot be increased arbitrarily. Larger transistor area leads to additional parasitic capacitance looking at the gate. From stability analysis, there are non-dominant poles looking at the gate of transistors M_3 (M_4) and M_7. Excessive parasitic capacitance can bring these poles nearer to the dominant pole, hence reducing the phase margin and endangering the stability of the OTA. The area of the transistors M_1-M_7 needs to be optimized for a balance trade-off between stability and noise performance.

Apart from that, input capacitance of M_1-M_2, C_{IN}, is related to the amplifier noise through equation (3.3).

$$\overline{v_{ni,amp}^2} = \left(\frac{C_1 + C_2 + C_{IN}}{C_1} \right) . \overline{v_{ni}^2} \tag{3.3}$$

$\overline{v_{ni,amp}^2}$ is the LN-AMP input referred noise while C_1 and C_2 are the feedback capacitors. Increasing gate area of M_1-M_2 arbitrarily leads to larger input capacitance and this would increase the input referred noise of the amplifier instead [20]. Thus area of the transistors M_1-M_2 need to be optimized to avoid jeopardizing the overall input referred noise.

Besides the flicker noise, the OTA design needs to be optimized for thermal noise to achieve optimum noise performance. The thermal noise of a MOS device looking at the gate is given by equation (3.4).

$$\overline{v_{d,MOS}^2} = 4kT\left(\frac{2}{3}\right)g_m \tag{3.4}$$

Substituting thermal noise source into equation 3.1, the input referred thermal noise of the OTA is revealed to be

$$\overline{v_{ni,thermal}^2} = \frac{16kT}{3g_{m1}} \left(1 + \frac{g_{m3}}{g_{m1}} + \frac{g_{m3}^{\ 2}}{g_{m1}g_{m5}} + \frac{g_{m7}}{g_{m1}} \right) \tag{3.5}$$

From equation (3.5), g_{m3} and g_{m7} are desired to be as small as possible while g_{m1} is preferred to be as large as possible. As low power design is required, an efficient use of current is needed to obtain a largest possible g_m at a given current. A MOS device can be biased in weak, moderate and strong inversion with the same biasing current using different sizing. The g_m of a MOS transistor can be described using EKV model [22], valid in all inversion regions, as depicted in equation (3.6).

$$g_m = \frac{\kappa I_D}{U_T} \cdot \frac{2}{1+\sqrt{1+4.IC}} \tag{3.6}$$

κ is the subthreshold gate coupling coefficient, I_D is the biasing current, U_T is the thermal voltage given by *kT/q*, and *IC* is the inversion conversion that describe the inversion region of the transistor. A MOS devices with *IC* larger than 10 is considered operates in strong inversion [21].

Thus from equations (3.5) and (3.6), it is desired that the input PMOS transistors M_1-M_2 are biased to operate in weak inversion to obtain largest possible g_m/I_D ratio and hence a more efficient use of current to optimize the input referred noise at the same time. This is realized by using a large $(W/L)_1$ so that the device operates in deep subthreshold region.

At the same time, as shown in equation (3.5), the devices M_3-M_7 need to have small aspect ratio to achieve low g_m. $(W/L)_3$ and $(W/L)_7$ need to be much smaller than $(W/L)_1$ to obtain a small g_m, forcing the devices M_3 and M_7 operating in strong inversion region. However, g_{m3} and g_{m7} cannot be reduced randomly in reality. As mentioned previously, there are non-dominant poles looking at the gate of M_3 (M_4) and M_7 which are given by g_m/C_g. C_g is the capacitance looking at the gate of transistor. Reducing the g_m drives the non-dominant poles to lower frequency and hence leads to lower phase margin. Therefore, the aspect ratio of M_3 and M_7 needs careful optimization to meet both input referred noise and stability requirements.

Another design aspect that needs to be taken care of is the output swing of the OTA. Equation (3.1) reveals that the transconductance of output transistors should be dominated by input transistor pair M_1-M_2 and hence smaller W/L ratio should be used. However at a fix biasing current, designing the output transistors with lower aspect ratio

leads to higher overdrive voltage. This in turn decreases the voltage headroom for output stage of the OTA [13][26].

Considering that the circuit is biased under 1.5V supply voltage, which is much lower than the nominal 3.3V supply for 0.35µm process, the output transistor sizes need to be optimized for adequate voltage headroom. Therefore the aspect ratio of the output stage transistors M_6, M_8, M_9, and M_{10} have to be fine-tuned to achieve a balanced trade-off between output voltage swing and input referred noise.

The sizes of the MOS devices in the LN- OTA are shown in Table 3.3.

Device	Dimension (µm/µm)
M_1, M_2	576 / 2
M_3, M_4, M_5	20 / 50
M_6	100 / 50
M_7	100 / 10
M_8	500 / 10
M_9	60 / 2
M_{10}	60 / 2
M_{11}	160 / 5

Table 3.3 Device dimensions of LN-OTA.

3.3 The Design of ADC

Following the amplification of the acquired ECG signal at the input stage, the analog signal is converted into digital output through a SA-ADC. The specifications, architecture and design of separate individual blocks in the ADC will be presented in this section.

In ADC specifications, the important specifications include clock frequency, sampling rate, resolution, number of bits and power consumption. To avoid aliasing, Nyquist sampling theorem is applied in deciding the sampling rate. Nyquist theorem states that the highest frequency which can be accurately represented is less than one-half of the sampling rates [24], as reflected in

$$f_N = \frac{1}{2} f_S \tag{3.7}$$

where f_N represents the signal bandwidth and f_S is the sampling rate. For sampling rate lower than double of maximum signal frequency, aliasing may arise causing distortion, where false frequency components that are not in the original analog signal, appear when the digital signal is converted back into analog signal.

As maximum ECG signal frequency is 150Hz, the sampling rate has to be at least 300Hz. In this design, the sampling frequency is set to be 500 Samples per second (S/s) to obtain a safety factor of greater than 3. The clock frequency is set to be 30 kHz while the number of bit is 11 bit. The overall specifications are summarized in Table 3.4.

Parameter	Value
Clock frequency	30kHz
Sampling rate	500 S/s
Number of bit	11 bit
Supply voltage	1.5V
Current consumption	As low as possible

Table 3.4 SA-ADC Specifications Summary.

3.3.1 ADC System Architecture

As discussed in Chapter 2, there are various kinds of ADCs can be used for different applications. For bio-application, low supply voltage and low power consumption are the main concerns in designing the building blocks, while the conversion speed is not so critical. Chapter 2 reveals that the successive approximation ADC (SA-ADC) has moderate complexity in digital circuitry with reasonable speed and resolution. Lower circuit complexity and lower speed translates into lower power consumption, thus successive approximation architecture is used in this ADC design. An 11 bit SA-ADC with 500S/s sampling rate is presented here.

The overall SA-ADC structure used in this design is shown in Figure 3.5.

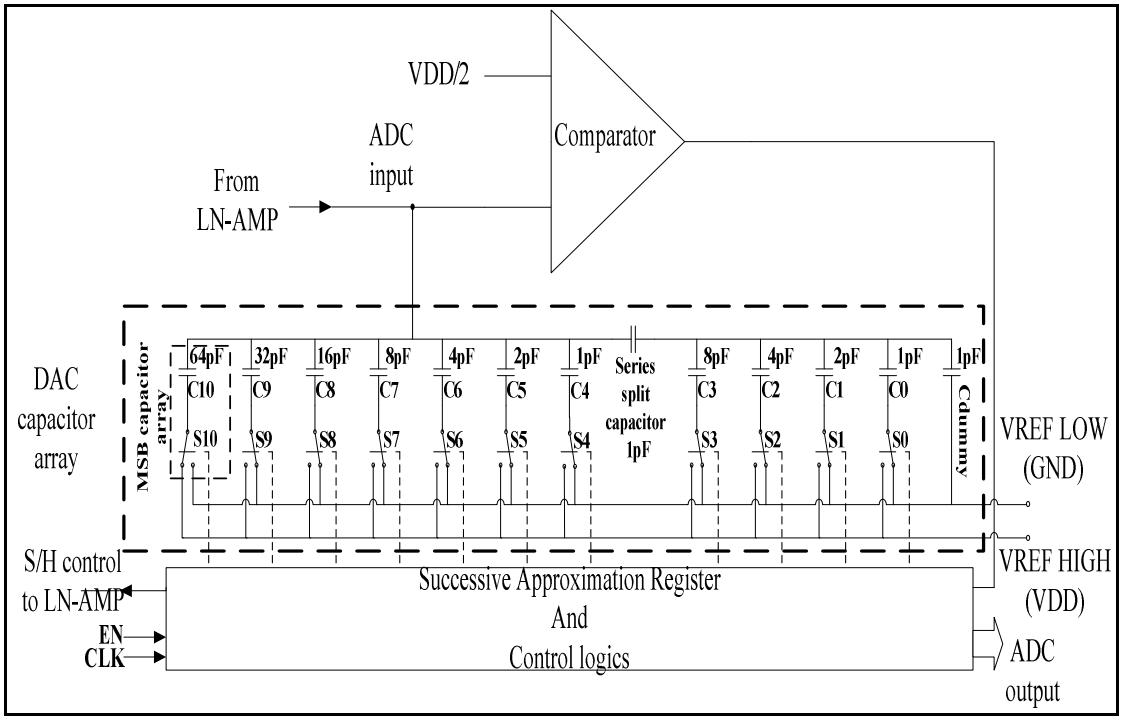


Figure 3.5 Overall SA-ADC structure.

The architecture used here is modified from the conventional structure. Conventional SA-ADC requires a supply voltage higher than $V_{THN} + V_{THP}$ whereas modified structures reported in [15] and [16] lack full V_{DD} input range and use huge capacitor to downscale the input signal, as discussed in Chapter 2. Due to the low supply voltage, it is desired that the ADC able to take in largest possible input, so to ease the requirement on the ADC resolution. A modified structure reported in [13] able to take in rail-to-rail input range. Hence the ADC architecture in this design adapted the structure reported in [13] with further modifications to conserve power consumption. These will be further discussed in the following section.

As seen in Figure 3.5, the main modifications for the ADC to acquire full V_{DD} input range is at the ADC input node. The ADC input node is connected directly to the Digital-

to-Analog Converter (DAC) capacitor array and comparator input. As long as the comparator reference voltage encompasses $V_{DD}/2$, the ADC can achieve rail-to-rail input. The comparator output is connected to the Successive Approximation Register (SAR) and control logics for further processing. Controls from SAR and control block are connected to comparator, DAC capacitor array and Sample-and-Hold (S/H) circuits.

The operation of the SA-ADC generally divides into three phases, which are reset, sampling, and conversion respectively. The operation can be illustrated in flow chart as shown in Figure 3.6. Variable N stands for the ADC resolution which is 11-bit in this design.

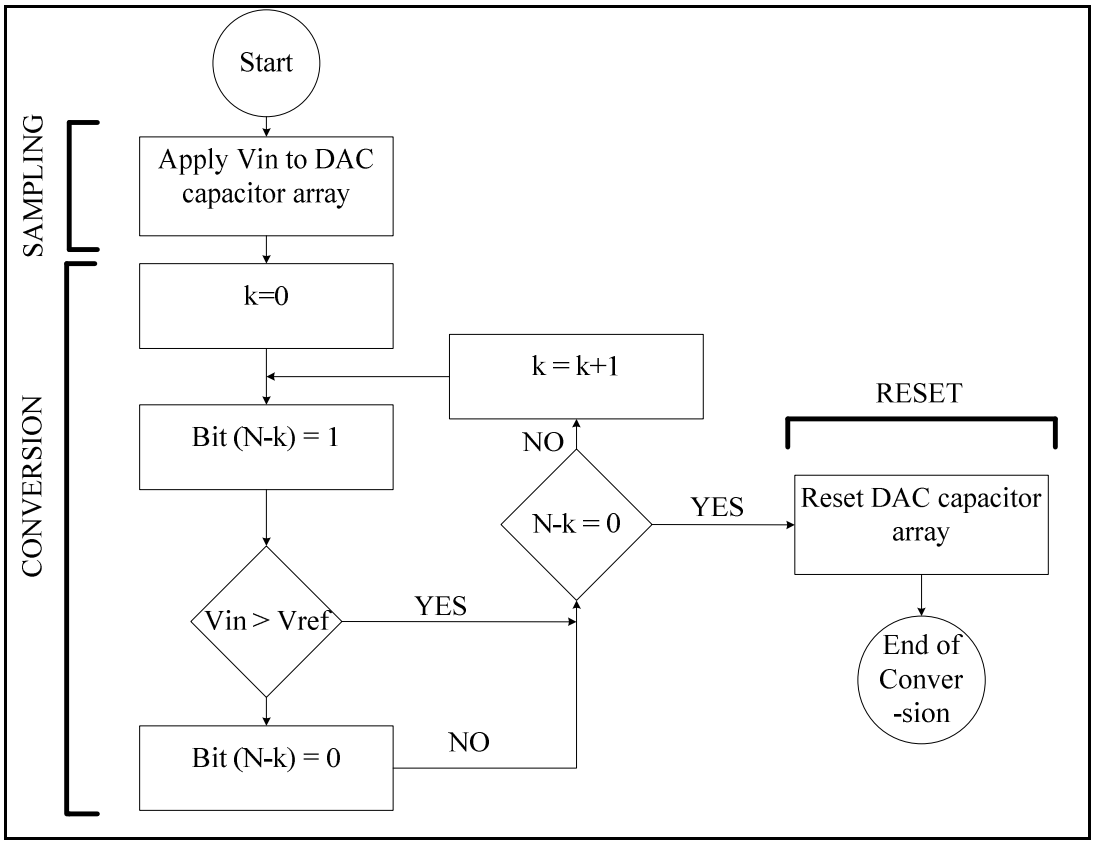


Figure 3.6 Flow chart of SAR operation.

The operation can be briefly described in the following. Firstly during the sampling phase, the holding capacitor, which is the DAC capacitor array, is charged to the LN-AMP output level. Prior to sampling phase, switch S10 is reset to V_{DD} while the rest of the switches are reset to ground.

Subsequently the voltage is held at the isolated ADC input node and the ADC conversion starts. During conversion phase, the conversion starts from the Most-Significant-Bit (MSB), proceeds on until Least-Significant-Bit (LSB). The held voltage at the DAC capacitor array is compared to reference voltage to decide '0' or '1' for the particular bit.

After bit decision at comparator, the output is fed into SAR and control logics to switch the DAC capacitor array for next bit conversion. The voltage at the input node successively approaches $V_{DD}/2$ to complete the overall A/D conversion.

After the conversion for all bits finishes, the DAC capacitor array will be reset for next round of sampling and conversion. As mentioned before, MSB capacitor will be reset to V_{DD} and the rest of the capacitors are reset to ground. In overall, 12 clock cycles are needed for the conversion and reset phase.

3.3.2 Sampling-and-Hold Design

In ADC design, a sampling-and-hold (S/H) circuit is inevitable as the analog input needs to be held for A/D conversion. However, additional S/H circuit would add to the current consumption of the overall system. To further conserve power consumption, the S/H circuit in this design is integrated into the output stage of the LN-OTA, as shown in Figure 3.7.

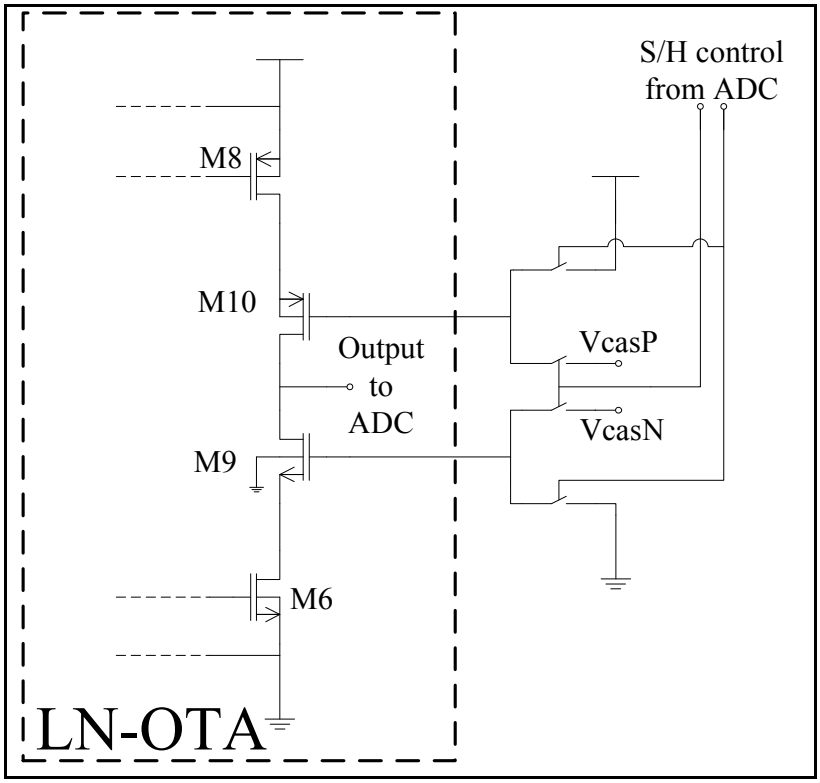


Figure 3.7 LN-OTA with integrated S/H function.

In Figure 3.7, the DC bias of output transistors M9 and M10 is connected to additional digital control. The S/H operation is completed by turning on and off transistors M9 and M10, in a way that these two transistors acting similar to switches. The control for S/H operation is connected from ADC digital control logics while the switches used in connecting the DC biasing are complementary switches. The overall operation is described next.

During sampling phase, the gates of transistors M9 and M10 are biased with ordinary DC biasing condition to VcasP and VcasN. The LN-OTA output is connected to the DAC capacitor array. As the DAC capacitor array also functions as the holding capacitor for

S/H operation, current in the LN-OTA output stage starts flowing to charge the holding capacitor to the desired voltage level.

During hold phase, gate of NMOS transistor M9 is biased to ground while PMOS transistor M10 to V_{DD}. Hence both output cascade transistors are turned off, similar to turning off the switches in S/H operation. The input node of the ADC is isolated and the charge is held on DAC capacitor array for A/D conversion. After the A/D conversion is completed, the overall S/H operation repeats again for next round of conversion.

In overall, there is no additional circuit needed, except some digital control circuitries. This greatly reduces circuit complexity for S/H operation and only digital power consumption is needed. Since the sampling rate in this design is set to 500S/s, which is considered rather low, the digital current consumption is significantly low compared to a dedicated DC current consumption in amplifier-based S/H circuits.

In addition, there is further current reduction in the LN-OTA. During conversion phase, the output transistors M9-M10 are turned off and thus no current is flowing through the output stage. As compared to constant DC current biasing, there is an 11% reduction in current consumption due to this dynamic nature.

However, one design consideration is that periodically switching the output stage will introduce error as the LN-AMP needs certain settling time when sampling phase starts. To tackle this issue, the sampling time is designed to be much longer than the hold time. In a complete S/H operation of 2ms, sampling phase takes 1.6ms while the rest 0.4ms is devoted to the conversion phase. Besides that, the output transistors M6 and M8-M10 are biased with larger current to improve the slew rate and reduce the output impedance. The settling error is minimized in these ways.

3.3.3 DAC Capacitor Array Design

In the successive approximation process, a DAC is required to generate the binary-weighted voltage for bit-decision. As there are various types of DAC available, a binary-weighted capacitor array is used in this design to cater for the SAR binary search algorithm. The main reasons of choosing a capacitor-based DAC are power conservation and better matching. A typical 11 bit DAC capacitor array is shown in Figure 3.8.

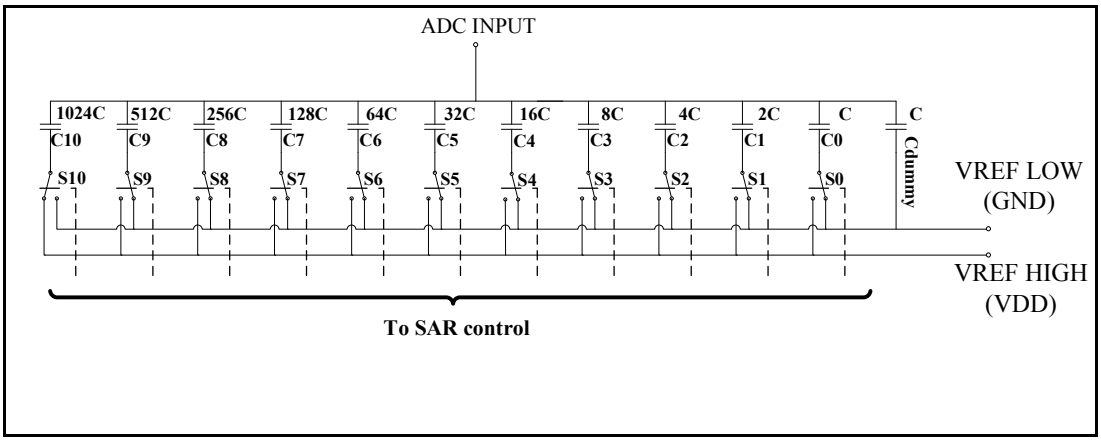


Figure 3.8 A typical 11 bit DAC capacitor array.

In Figure 3.8, C is the unit capacitance and a dummy capacitor is needed to fulfill binary weighted requirement. Total capacitance needed would be 2^{11}C where individual capacitor varies in order of 2^n with n increases from 0 to 10 in this design.

The binary-weighted capacitor array works with charge redistribution principle where the capacitors are simply acting like voltage divider [10][27]. During conversion phase, the capacitors are switched to high or low reference voltage causing the charges redistributed among the capacitors. Hence the voltage held at the ADC input will swing

in binary weighted step, successively approaches $V_{DD}/2$ to complete the overall conversion.

From Figure 3.5, the DAC capacitor array is connected to the comparator input for bit-decision. Hence the input parasitic capacitance of the comparator forms part of the DAC capacitor array introducing error in the binary weighted voltage step. To minimize this effect, the unit capacitance has to be significantly larger than the parasitic capacitance. In this design, the unit capacitance is set to 1.3pF while the comparator parasitic input capacitance is less than 100fF.

However, using a large unit capacitance will cause overall area increase exponentially. With 1.3pF unit capacitance, a total of 2048×1.3pF capacitance area is needed where this is nearly impossible if a fully integrated chip without off-chip components is desired. For this reason, a series split capacitor array is implemented in the design as shown in Figure 3.9.

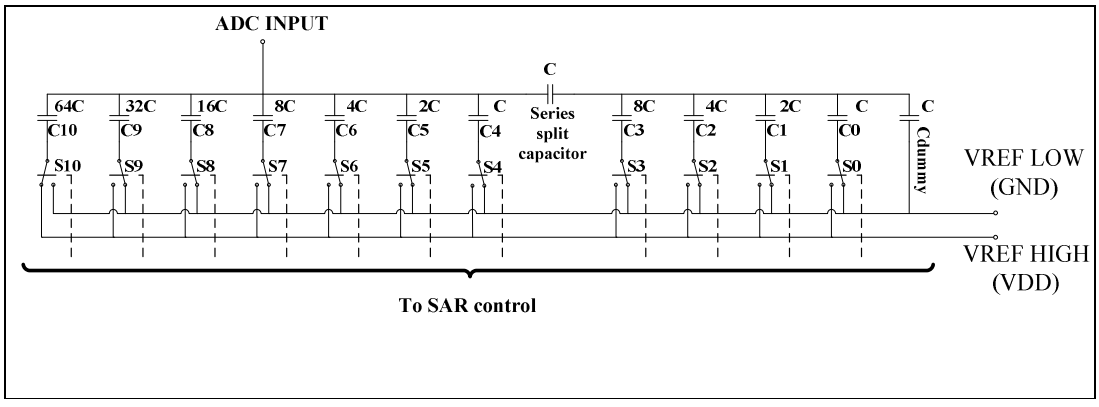


Figure 3.9 An 11 bit series split DAC capacitor array.

The DAC capacitor array is split into two sub-arrays with an attenuation capacitor in between. The series split capacitor scales down the lower bit capacitors from LSB capacitor C0 to C3 such that the series combination of attenuation capacitor and lower bits array still approximate to unit capacitance C. Thus the binary weighted voltage division is still equivalent to the typical architecture while total capacitor area is greatly reduced.

Conventional binary weighted DAC capacitor array shown in Figure 3.8 and Figure 3.9 is insensitive to stray capacitance but energy inefficient [28-29]. With low power design in consideration, a further modification was done to the DAC capacitor array where "split" capacitor array architecture is used in this design. Not to be confused of the series split capacitor array where a series connected attenuation capacitor is used; the main idea is to split the MSB capacitor into a sub-array which is identical to the rest capacitor array [28-29], as shown in Figure 3.10.

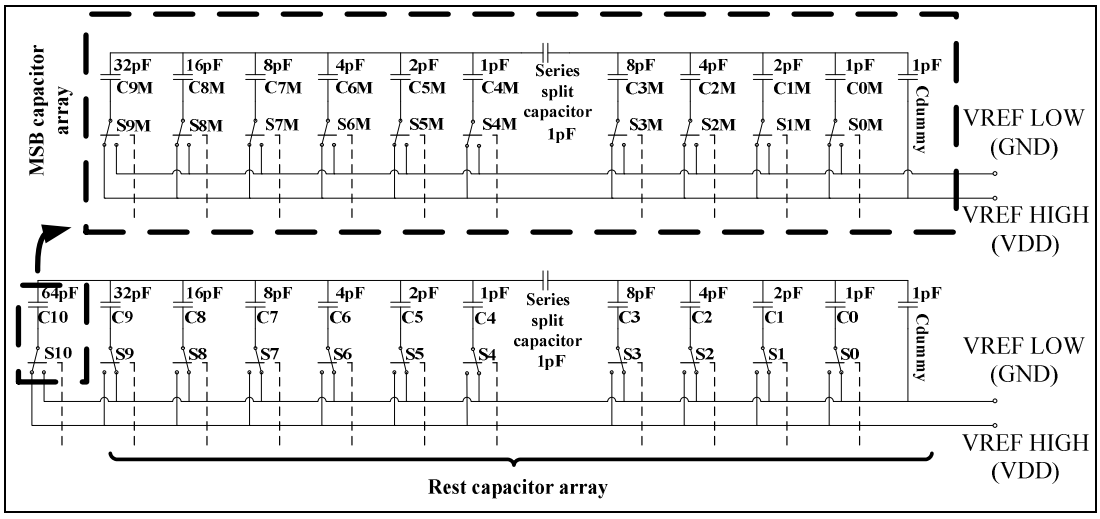
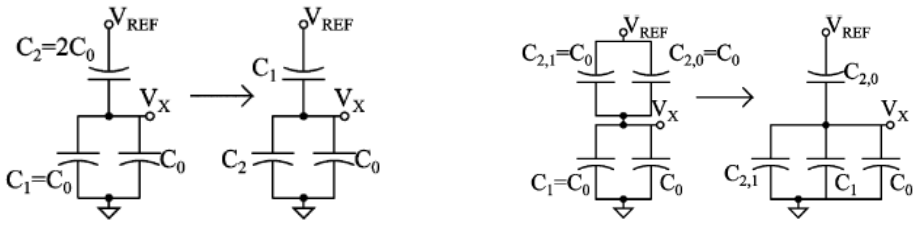


Figure 3.10 "Split" structure with MSB sub-array and the rest capacitors sub-array.

In Figure 3.10, MSB capacitor C10 is split into another sub-array which is exactly the same with the rest capacitor array from C9 to Cdummy. Both arrays are implementing the series split capacitor architecture as mentioned previously. The total capacitance used in this approach would be the same with the conventional binary-weighted capacitor array. However since a series split capacitor is added in each array, there is additional capacitance of 16C needed.

This modification in DAC capacitor array structure aims to reduce the energy consumed by the capacitor switching during conversion phase. Less capacitance is involved in switching activities for this modified structure as opposed to conventional approach, hence less energy consumption as illustrated in the following example.



Conventional Approach "Split" Approach

Figure 3.11 Comparison of different approach for down conversion example.

In this 3 bit capacitor array down conversion example shown in Figure 3.11, only one unit capacitance in MSB sub-array is switched downwards in "split" approach. In contrast, two unit capacitors of MSB capacitor need to be switched downward while one unit capacitance is switched upwards in conventional approach. After switching, both approaches have identical capacitor array.

By greatly reducing switching activities and capacitance involved, up to 37% switching energy could be saved in the "split" approach. Detail calculation on energy saving is shown in [28]. In addition, less capacitance involves in the conversion would help to increase speed and improve DNL performance. The main contradiction is that there are more connections and additional control. This introduce more complexity in digital circuitries and hence slight increase in power consumption. However, overall power consumption will still be conserved considering large reduction in switching activities.

3.3.4 Comparator Design

The comparator is an essential block in all types of ADC as it serves the important function in bit-decision. In this design, the overall comparator architecture consists of a pre-amplifier, a regenerative latch, a SR latch and a clock control block. The design is basically using the regenerative structure, as presented in Figure 3.12.

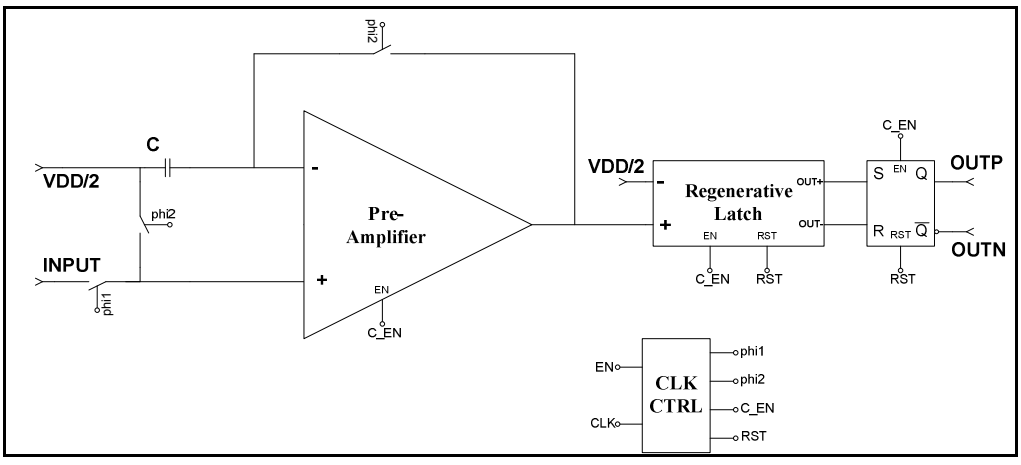


Figure 3.12 Overall comparator architecture.

The regenerative latch is a synchronous clocked latch that amplifies input signal to a substantial differential level. However, the regenerative latch by itself is not able to achieve the resolution required for the ADC. For an 11bit ADC with 1.5V full V_{DD} input range, the comparator must be able to detect a voltage difference as low as 700μV.

Hence the input pre-amplifier is needed to amplify the input signal to a significant magnitude before the regenerative latch and thus increase the minimum detectable difference for the latch. In addition, adding a pre-amplifier greatly reduce the regenerative latch time to develop the required logic level as the input level to latch is already amplified. This would increase the overall comparator speed in bit-decision.

Besides that, the input preamp also helps to reduce the kickback noise with referred to the comparator input, which is connected to the DAC capacitor array. Kickback noise is generated when the latches are clocked to switch between different states and the noise is injected from the latch to the input of comparator. As the LSB of the ADC is only 732μV, the kickback noise may interfere the sensing at the comparator input. By using a pre-amplifier as the input stage, the kickback noise is reduced by the gain of the pre-amplifier when referred back to the comparator input.

Basically the input pre-amplifier is an ordinary current-mirror OTA similar to the LN-AMP design. The architecture of the pre-amplifier is shown in Figure 3.13. Since an open loop approach is used during comparison phase, the pre-amplifier achieves very high gain helping to improve the resolution of the comparator. However, very large gain also means small offsets in the pre-amplifier can easily saturate the output of the comparator. Thus an offset cancellation scheme is needed to mitigate this problem. The operation of the comparator can be described in the Figure 3.14.

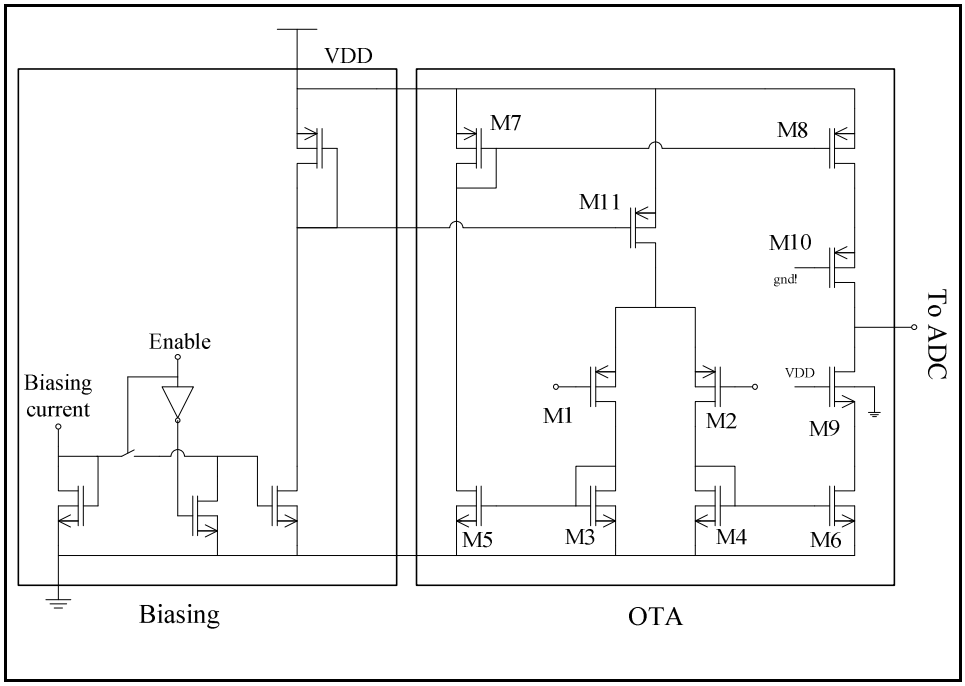


Figure 3.13 Comparator pre-amplifier circuit.

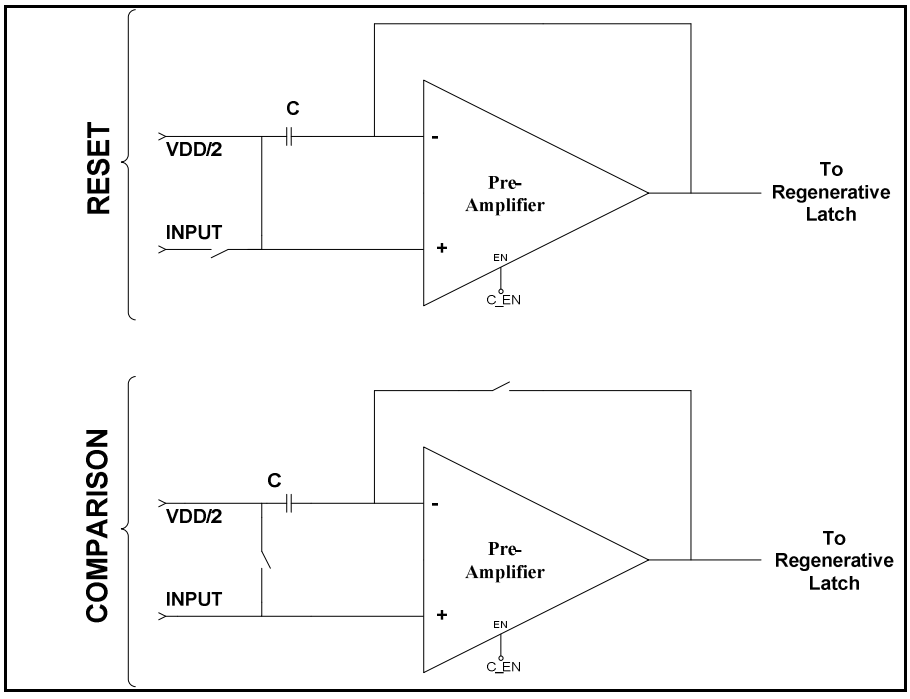


Figure 3.14 Input offset cancellation of comparator pre-amplifier.

In every clock cycle during the ADC conversion phase, the comparator pre-amplifier is reset to complete the input offset cancellation operation. In the first half clock cycle as the reset phase, the pre-amplifier is set to a closed loop form. The output offset of the comparator preamp is sampled and stored in the pre-amplifier input capacitor, C as shown in Figure 3.14. Then for the next half clock cycle as the comparison phase, input to the comparator will be offset by the voltage stored in the storing capacitor C and thus correcting the amplified output signal.

After comparison for the present bit, the comparator is reset and repeats the input offset cancellation operation again for next bit-decision. Since the offset is stored when the pre-amplifier is closed-loop, larger amplifier gain will give more accurate results. The main device dimensions of the pre-amplifier circuit are included in the following table.

Devices	Dimension (um/um)
M_1, M_2	48 / 1
M_3, M_4, M_5	4 / 5
M_6	8 / 5
M_7	5 / 3
M_8	10 / 3
M_9	60 / 2
M_{10}	64 / 4
M_{11}	2 / 10

Table 3.5 Device dimensions of Comparator Pre-amplifier.

The circuits of the regenerative latch and the SR latch are shown in Figure 3.15 and Figure 3.16 respectively. The regenerative latch design has a gain of 3 to 4 and is reset every clock cycle to further reduce the latch time. Hence, the SR latch is used here to hold the output at the rail-to-rail voltage level a clock cycle. Apart from that, as open loop approach is used in the pre-amplifier, a certain amount of time is needed for the output signal of the pre-amplifier to build up. Thus a delay of approximately 3μs is applied to the regenerative latch and the SR latch to turn on both the circuit.

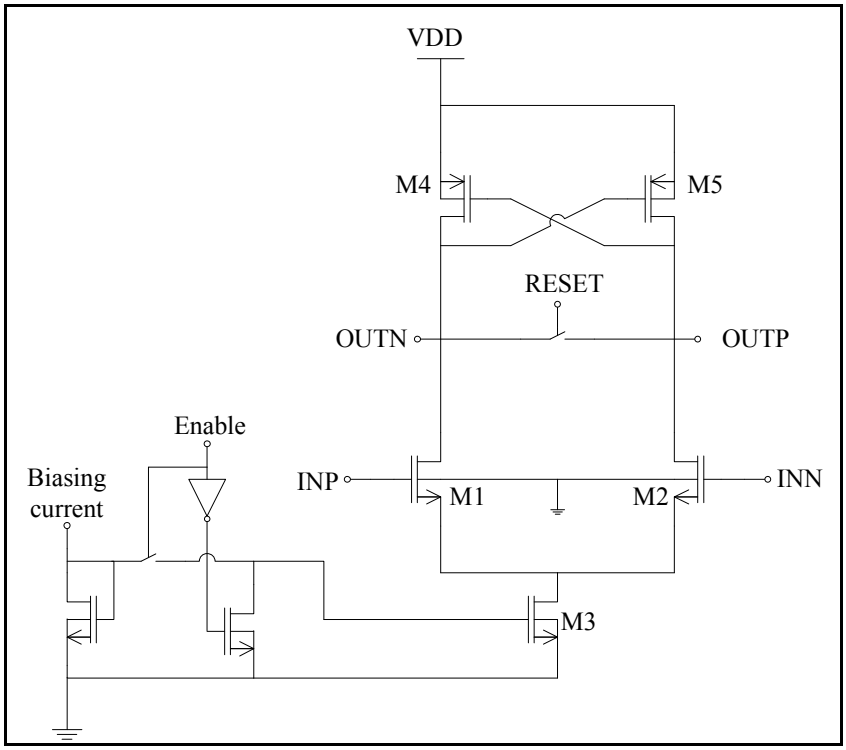


Figure 3.15 Comparator regenerative latch.

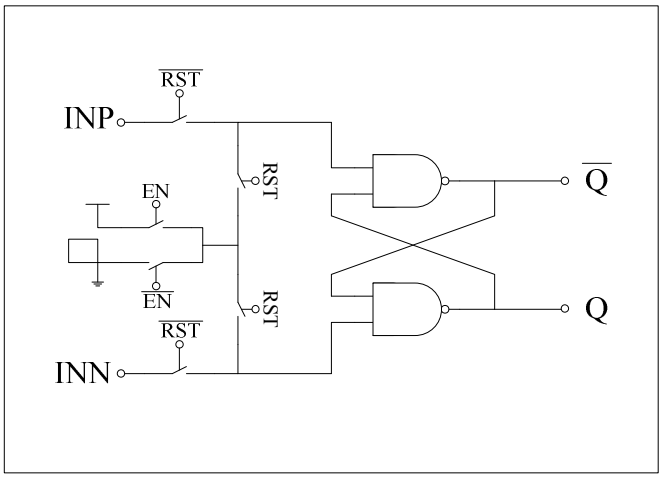


Figure 3.16 SR latch.

Besides that, the whole comparator except the biasing circuit is switched off during sampling phase of the SA-ADC and only turned on during ADC conversion phase. By implementing this dynamic nature, the current consumption of the overall system can be further reduced. The MOS device sizes of the comparator regenerative latch are shown in Table 3.6. As for the SR latch, the circuit is made of standard digital circuits provided by the foundry.

Device	Dimension (um/um)
M_1, M_2	16 / 4
M_4, M_5	4 / 10
M_3	32 / 5

Table 3.6 Device dimensions of comparator regenerative latch.

3.3.5 SAR and Digital Control Design

The Successive-Approximation-Register (SAR) and digital control circuitries play the important role in determine the value of each bit from MSB to LSB in a sequential manner based on the comparator output. At the same time, these circuits control the switching of DAC capacitor array for A/D conversion, overall sampling-and-hold (S/H) operation, and clock distributions to all other blocks in SA-ADC. The SAR control portion is primarily made of shift register, control logics, multiplexer and serial output latch, as shown in Figure 3.17.

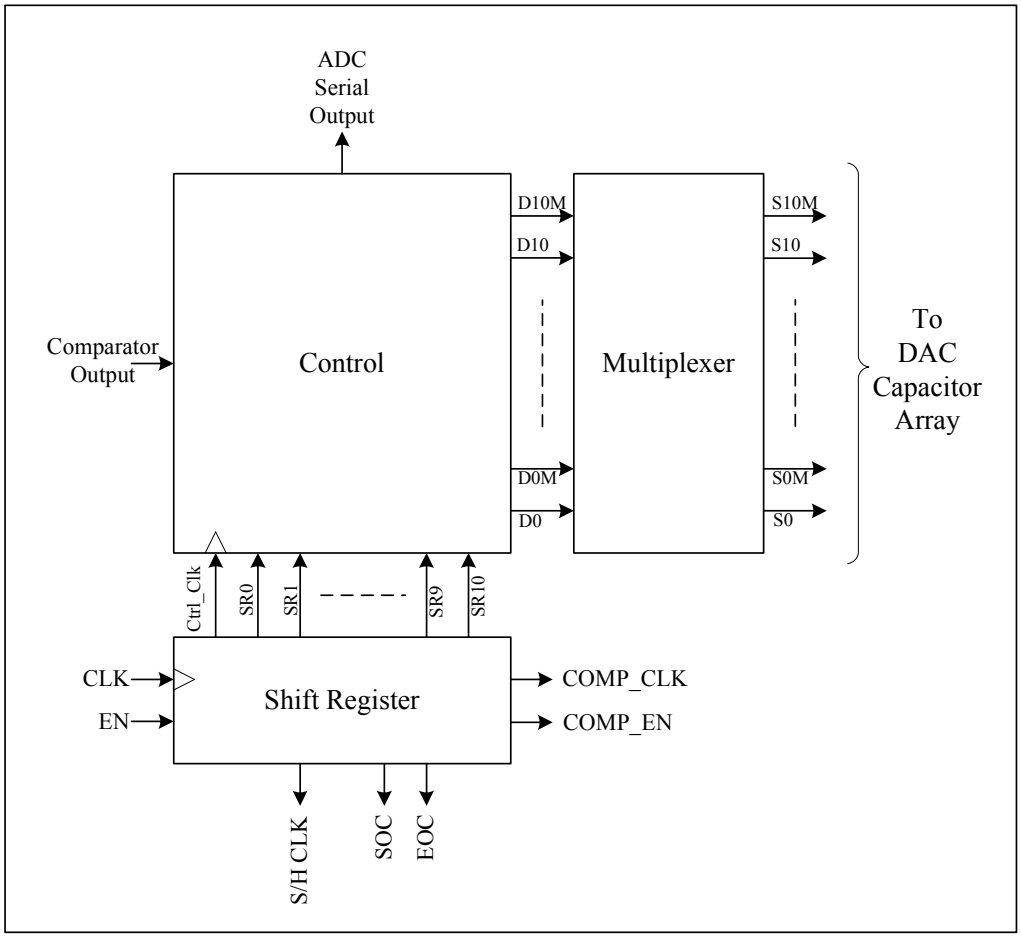


Figure 3.17 SAR and control logics digital block.

Basically, the shift register acts as a counter which counts cycles to complete the successive approximation conversion with a clock feeding in the shift register. In this design, the shift register takes in an external clock and starts to count automatically when it is enabled. The shift register is designed to control all clocks in the ADC and thus controlling S/H operation, A/D conversion, and comparator input offset operation. The structure of shift register is shown in Figure 3.18.

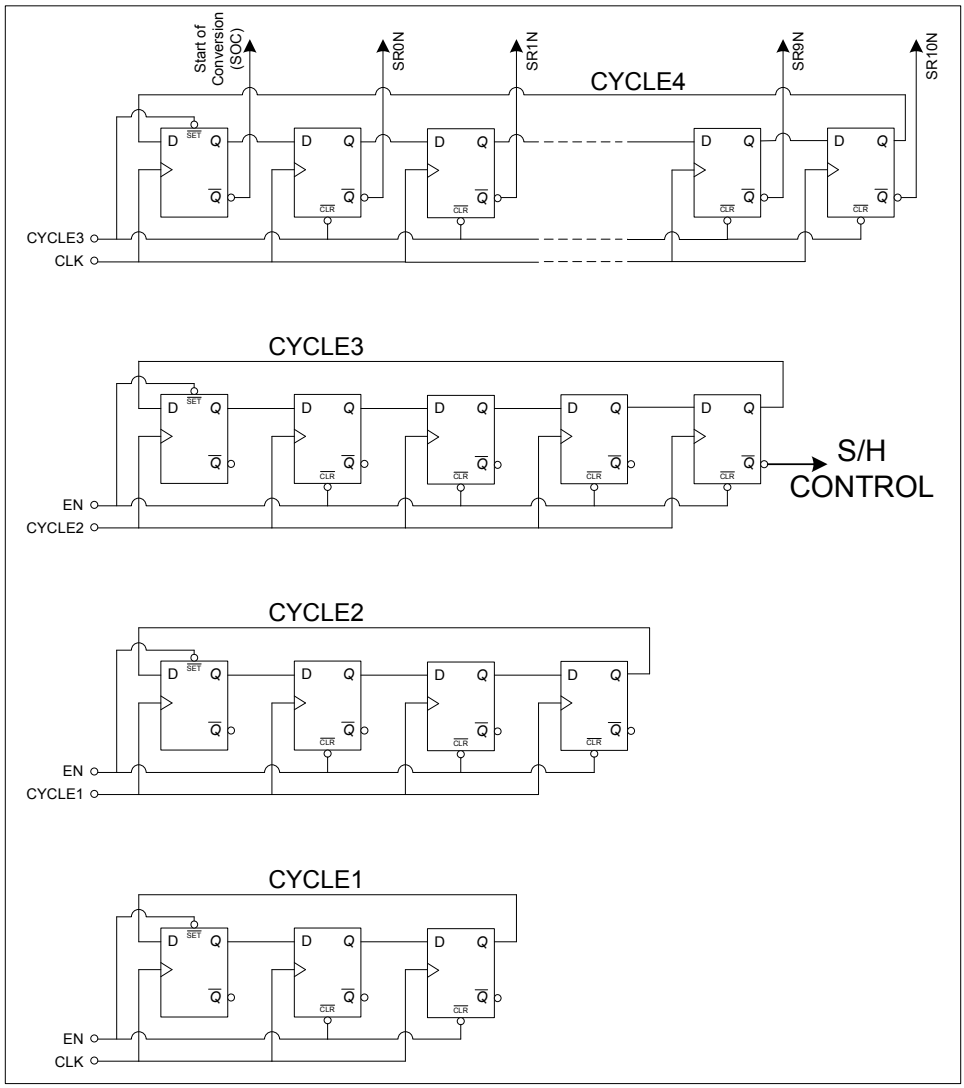


Figure 3.18 Shift register structure.

The shift register is basically made of D flip-flops. An enable signal will reset the shift register and start counting. As the sampling phase needs much longer time than conversion phase in this design, a complete S/H operation is designed to be 60 clock cycles with 48 cycles assigned to the sampling phase and 12 cycles assigned to the conversion phase.

However, letting the ADC active all the time will make the overall power consumption increase substantially. Therefore a modification is made to the shift register whereby only block CYCLE1 is active all the time. Block CLCYE1 enables block CYCLE2 while block CYCLE3 is controlled by block CYCLE 2. Block CYCLE4 is enabled by block CYCLE3 and thus starts the count of 12 clock cycles for A/D conversion. In this way, switching activities are minimized and power consumption is conserved to the greatest extent.

Outputs of the D flip-flops in block CYCLE4 are tapped to the control and multiplexer block which in turn controls the DAC capacitor array. Total 12 clocks cycles are needed for A/D conversion. 11 bit conversion takes up 11 clock cycle while the last clock cycle is to signal end-of-conversion (EOC) and reset the whole DAC capacitor array.

As for the control unit, it is basically a D flip-flop that reads in the comparator output and holds the logic for the present bit. The output of the control unit will switch the corresponding capacitor of the DAC capacitor array through the multiplexer. There are eleven multiplexer units representing 11 bits. The outputs of the shift register tap to the multiplexer units to turn on the right unit so that the output from control unit can be fed into the corresponding capacitor switch. The structure is shown in Figure 3.19.

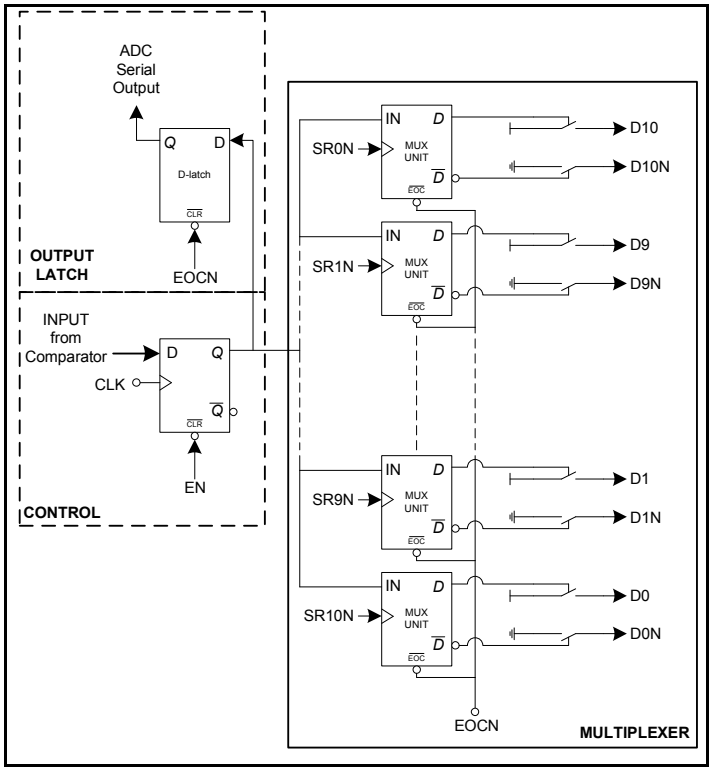


Figure 3.19 Control and multiplexer structure.

Taking MSB for example, the control unit reads the first output of the comparator and decides the MSB bit to be high or low. SR0N from shift register turn on the corresponding multiplexer unit to feed the MSB bit to the MSB capacitor. The MSB capacitor will be switched to the corresponding logic and held until conversion completed. Then the comparator will start to compare to decide next bit and the process will continue until the full conversion cycle is done.

In this design, the output of the ADC is set to be serial output to further reduce the power consumption. The main advantage in doing so is the large reduction in digital circuitries complexity. As shown in Figure 3.19, only one D flip-flop in control unit and single output latch are needed. The switching activities are greatly reduced, hence

reducing digital power consumption. In comparison, parallel output would at least require 11 output latches which increase the power consumption exponentially.

However, one disadvantage is that there are more post processing works need to be done on ADC output to convert the serial output into relevant output code, as compared to the parallel output. It is possible to solve this issue as the post processing works are in digital domain and mainly done at base station processor. This will be further discussed in Chapter 6.

3.4 Design summary

The overall specifications for the ECG signal acquisition chip are summarized in the following table. Simulation results and measurement on the fabricated chip will be further discussed in the following chapters.

Block	Parameter	Value
LN-AMP	Gain	200 V/V
	Bandwidth	<0.3 Hz to >150 Hz
	In-band input referred noise	< 1.5 μV_{rms}
SA-ADC	Clock frequency	30 kHz
	Sampling rate	500 Hz
	Number of bits	11 bit
Overall	Supply voltage	1.5V
	Current consumption	As low as possible

Table 3.7 Overall design specifications.

CHAPTER 4 Overall System Implementation and Verification

This chapter elaborates on the implementation of overall system into physical layout for chip fabrication. Layout design considerations will be illustrated in minimizing undesired effects on the design. In the latter section, post-layout simulations were done to verify the circuit performance before the design was sent for tape-out. Some discussions on the simulation results are included as well.

4.1 Layout Design

The layout of the design was implemented in AMS 0.35µm CMOS standard technology process. Final layout to be sent for fabrication includes an overall integration system circuit and three test blocks. The overall integrated acquisition system consists of the LN-AMP and SA-ADC as illustrated in Chapter 3. Meanwhile, the test blocks, including a LN-AMP, a LN-OTA and a SA-ADC are meant for individual circuit testing to extract performance for each individual circuit.

Various layout design strategies were employed to minimize parasitic effects with references to [10], [17], [24-25] and [30-33]. Details on the layout techniques are to be discussed in the following sections.

4.1.1 Low Noise Amplifier (LN-AMP) Layout Design

In LN-AMP floor plan design, the LN-AMP is divided two main parts which are the capacitors network and the LN-OTA. The layout of the LN-AMP is shown in Figure 4.1.

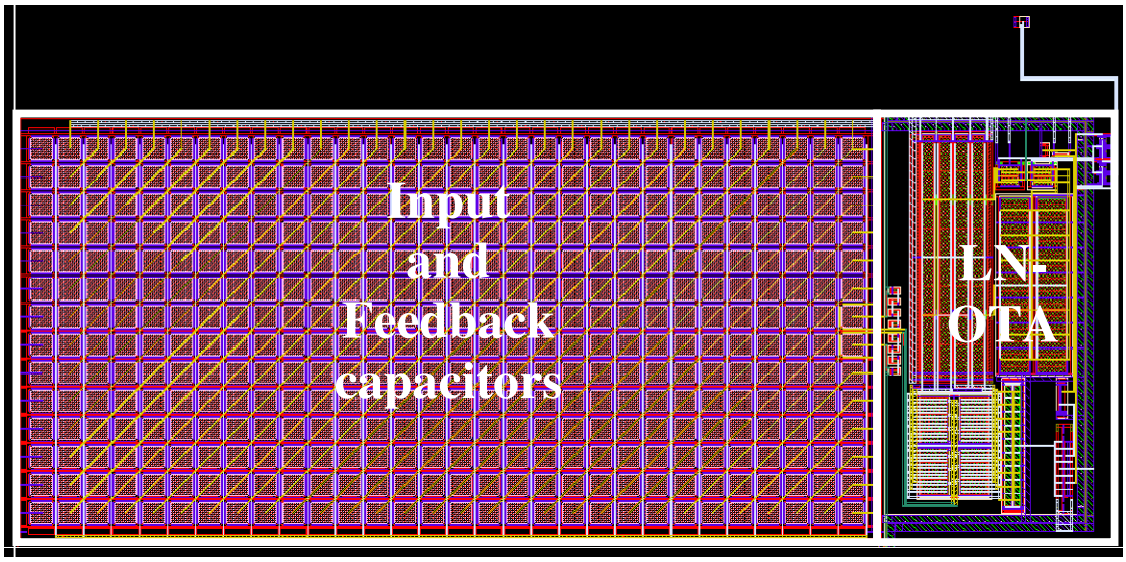


Figure 4.1 LN-AMP layout.

As the ratio of input capacitor C_1 and feedback capacitor C_2 decides the gain of the LN-AMP, these two capacitors need to be well-matched. Hence, a capacitor network that includes both capacitors is used where capacitor C_1 is split into 200 unit capacitors identical to capacitor C_2, with 0.3pF for each unit capacitor.

Apart from that, the capacitors at the edge of the capacitor network may suffer from etching effect, causing the area of these capacitors deviates from those unit capacitors that are completely surrounded. At the same time, these capacitors at the edge may also suffer from extra interference as compared to those inner unit capacitors. Therefore, dummy capacitors were added to surround the whole capacitor network.

The overall capacitor network is shown in Figure 4.2. As C_1 is the input of the LN-AMP that takes in very weak analog signal, guard-ring needs to be added to surround the capacitors. The main purpose is to minimize interference and noises couple to the capacitors. Guard-ring basically is the P-substrate contact or N-well contact, which usually connected to a clean power supply to couple the interference to the V_{DD} or ground.

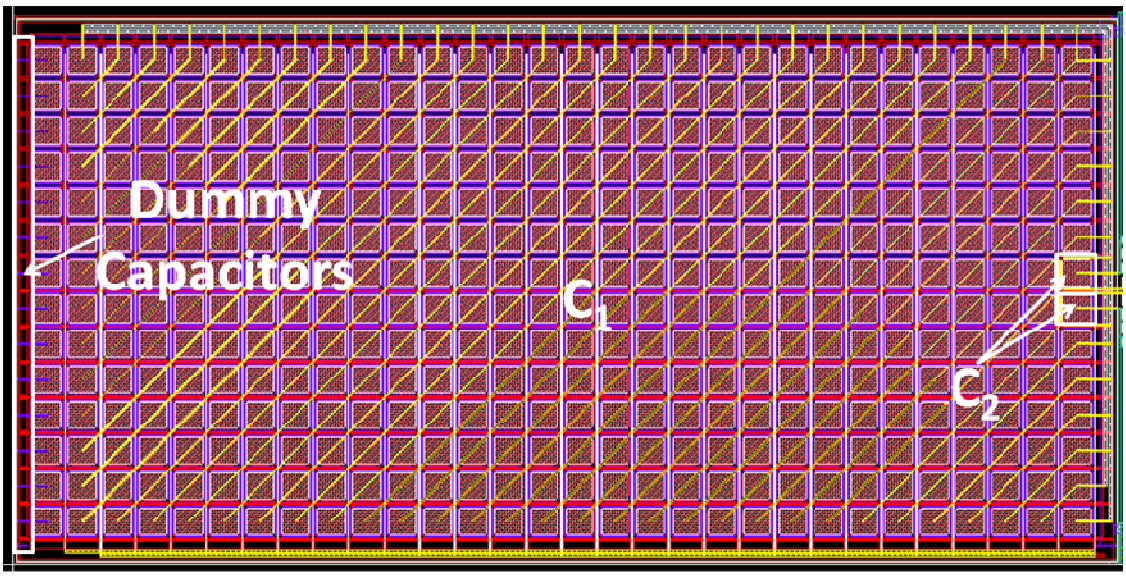


Figure 4.2 Capacitor network of the LN-AMP.

As for the second main block, the LN-OTA mainly consists of MOS transistors. The main concerns of design are in the input transistor pair and the current mirror transistors. This is due to the input transistors is a differential pair where both transistors must be identical to each other to minimize any mismatch that may lead to input offset or distortions. As for the current mirror transistors, the ratio between the mirror pair is important.

To ease the difficulty in floor planning, multi-finger transistors were used. The input differential pair transistors were drawn in inter-digitized structure to improve the matching. Same approach is adapted to the current mirror transistors. As mentioned in the chapter 3, the LN-AMP is amplifying very weak signal and need to have very low input referred noise. Thus a guard ring was added surrounding the OTA to minimize any noise or interference from the surrounding environment. The detail LN-OTA layout is shown in Figure 4.3.

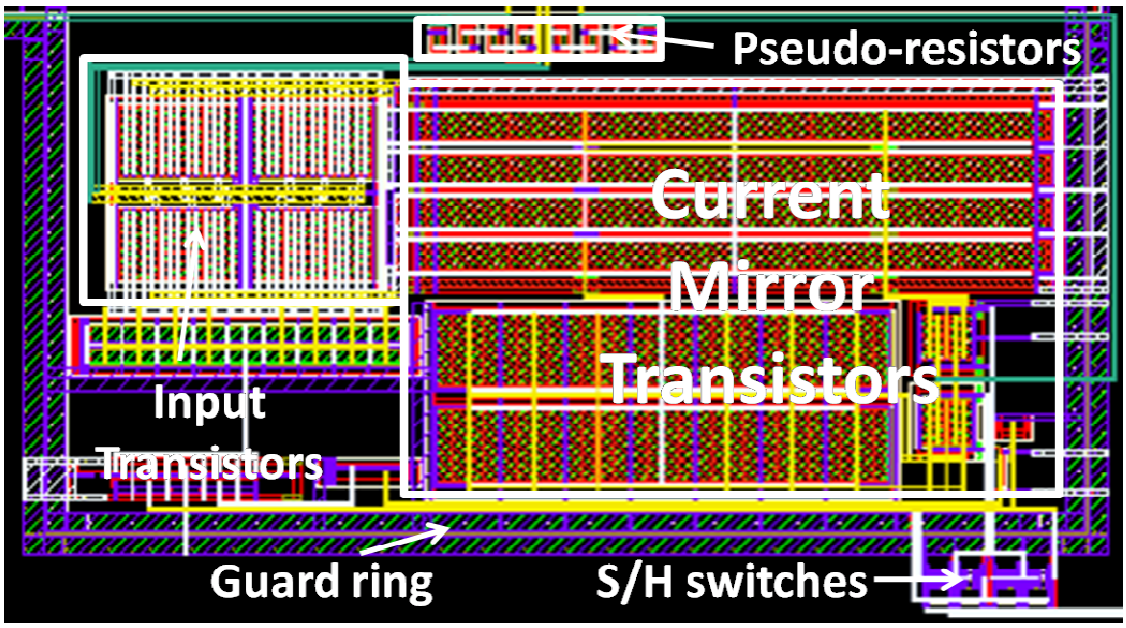


Figure 4.3 LN-OTA layout.

Meanwhile, the S/H controls and switches were put further away from the LN-AMP input and outside the LN-OTA guard ring. This is due to the switching activities is considered very noisy and may cross-coupled to the OTA.

4.1.2 SA-ADC Layout Design

The SA-ADC primarily comprises three main blocks, which are the comparator, DAC capacitor array, and SAR-control digital circuits. The overall layout floor plan is shown in Figure 4.4.

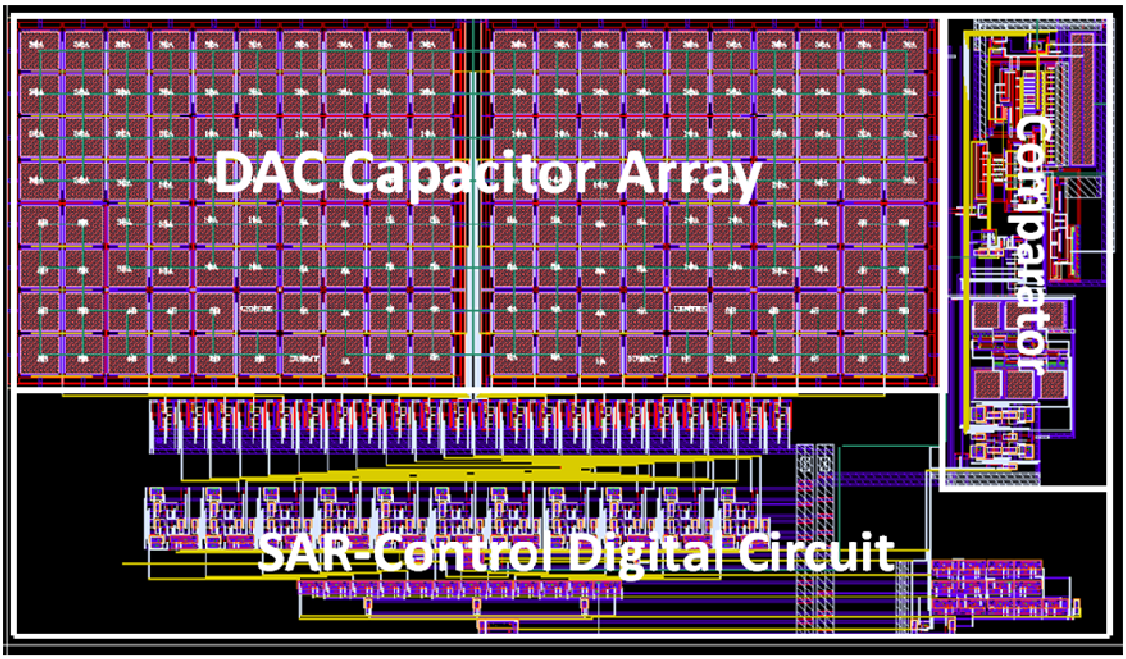


Figure 4.4 SA-ADC layout.

There are three small blocks in the comparator which are the pre-amplifier, regenerative latch and the SR latch. Due to similar structure to LN-OTA, the pre-amplifier layout is drawn using the same design strategies. The input transistor pair and current mirror transistors are drawn in inter-digitized structure with multi-finger transistors. Overall comparator is surrounded by guard-ring to reduce interference to the comparator input. The switches and clock control block are placed outside of the guard-

ring at the comparator output since the comparator output is digital in nature. The overall comparator layout is shown in Figure 4.5.

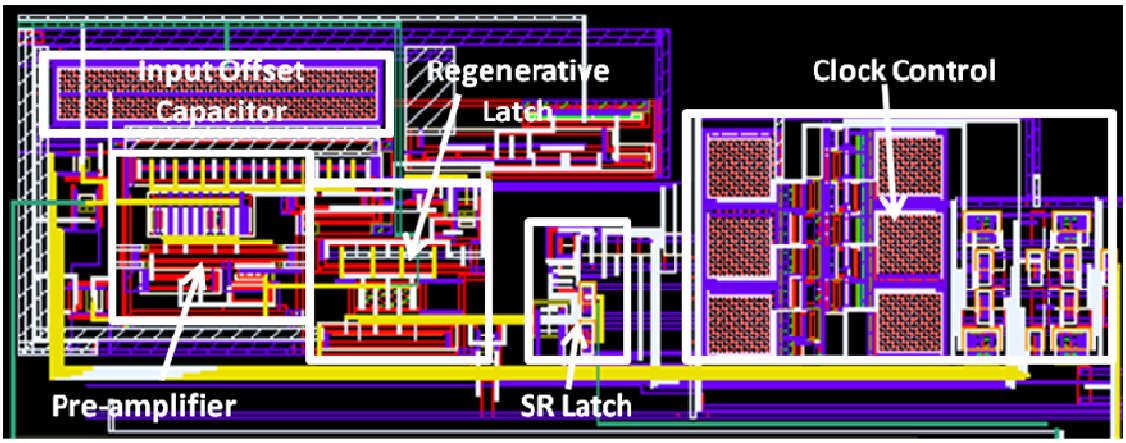


Figure 4.5 Comparator layout.

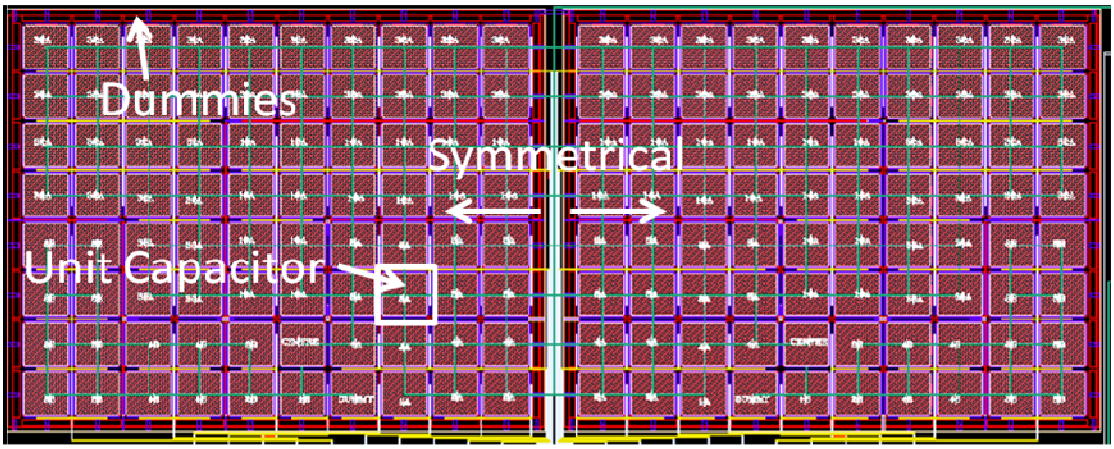


Figure 4.6 DAC capacitor array layout.

For the DAC capacitor array, it is also adapting the same design consideration with the capacitor network in LN-AMP. As the capacitor array is binary-weighted in nature, the capacitors are built from unit capacitors to achieve better matching and more accurate

ratio. The unit capacitor size is chosen to be 36µm × 36µm equivalent to 1.3pF. A larger capacitor helps to improve the matching error as larger area has smaller deviation.

The DAC capacitor array is also surrounded by dummy capacitors to reduce etching effect to the effective capacitor area between center units and boundary units. As there are two arrays of capacitors, both arrays and connections are made to be as identical and symmetrical as possible. This would help in minimizing errors and mismatch as the parasitic capacitance will be largely symmetrical and binary weighted as well.

Besides that, higher level metal is used as interconnects due to lower parasitic capacitance to substrate. The whole capacitor array sits on the N-well and surrounded by guard-ring to further reduce coupled substrate noise.

As for the digital portion, the SAR and control logic circuits should be drawn as compact as possible to save chip area. The orientation of metals should be taken care for better routing. For example, metal 1 is used for horizontal routing while metal 2 is used for vertical routing. Lower metal is preferred in routing as this would help in high level integration system floor plan. Wider metal line and extra vias should be used for power line connections.

Another concern is that the shift register should be placed at an ideal location as it distributes all the clock controls to whole system. Clock trees are used to reduce delays along the long clock signal lines. However, delays may not be as critical in this design since the clock frequency is rather low.

4.1.3 Integrated System Floor Plan Design

The overall integrated system layout is shown in Figure 4.7. As the overall system is a mixed signal design, the overall floor plan needs to be well taken care to avoid contamination of analog signal by the switching activities in digital circuits. An example of such interference is termed clock feed-through where the clock activities are coupled into the analog circuits through substrate.

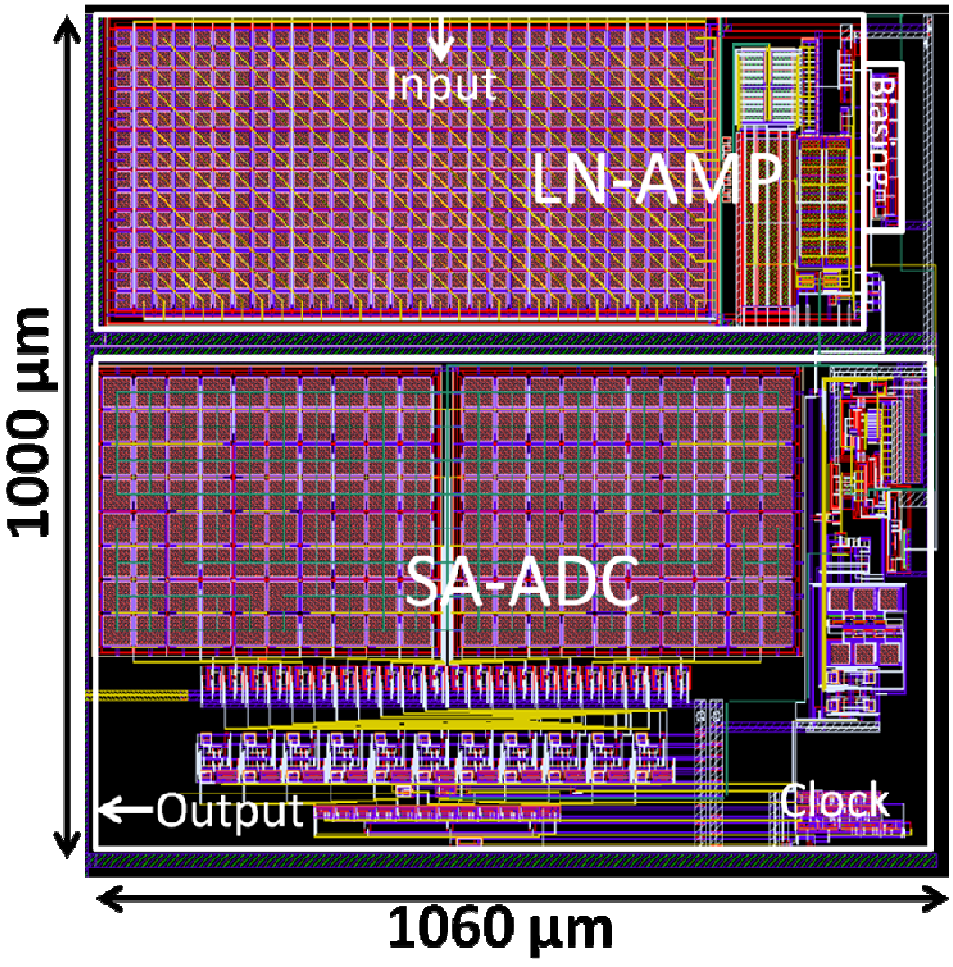


Figure 4.7 Overall integrated system layout.

In this design, the analog portion represented by LN-AMP is separated from the digital circuitries, which is the SA-ADC. Guard ring are laid in between these two blocks to provide shielding and protection to the analog circuits. The guard ring should be connected to a clean power supply to couple the digital noise to the power supply. In this case, the guard ring is connected to the ground supply.

In addition, since the input signal is very weak, the input terminal is located far away from the digital portion as shown in Figure 4.7. The digital output and clock input is also distant away from the analog portion.

Overall integrated system is measured to be 1000µm by 1060µm.

4.2 Post Layout Simulation

Subsequent to layout implementation, the performance of the design was verified in post layout simulation. The idea is to include parasitic effects that may appear in the physical chip into the design. As the simulation model before layout design does not attach these parasitic, the post-layout simulation results would give a better estimation on the performance of the design.

4.2.1 LN-AMP Simulation Results

Simulation was done to extract the frequency response of LN-AMP. The magnitude response is shown in Figure 4.8 while the phase response is shown in Figure 4.9. The gain of the LN-AMP is exactly 200V/V which is equivalent to 46dB. The high pass 3dB cut-off frequency is about 0.13Hz while the low pass 3dB cut-off frequency is about

192Hz. This would cover the ECG signal bandwidth although the high pass 3dB cut-off frequency is still slightly higher than specifications.

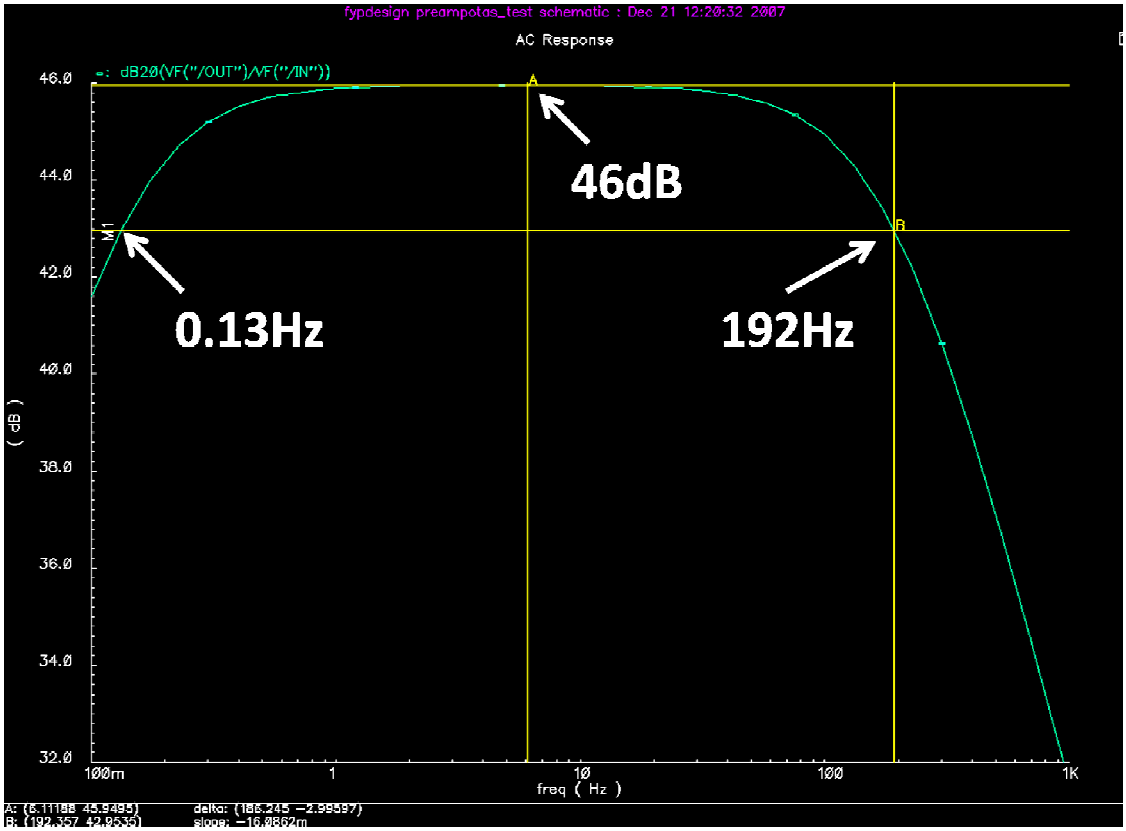


Figure 4.8 Magnitude response of LN-AMP.

The unity gain phase margin extracted from the loop gain response is about 50°, which should be just sufficient for stability. The phase margin is trade-off to achieve an optimized input referred noise performance, which will be shown in the simulation results of the later part.

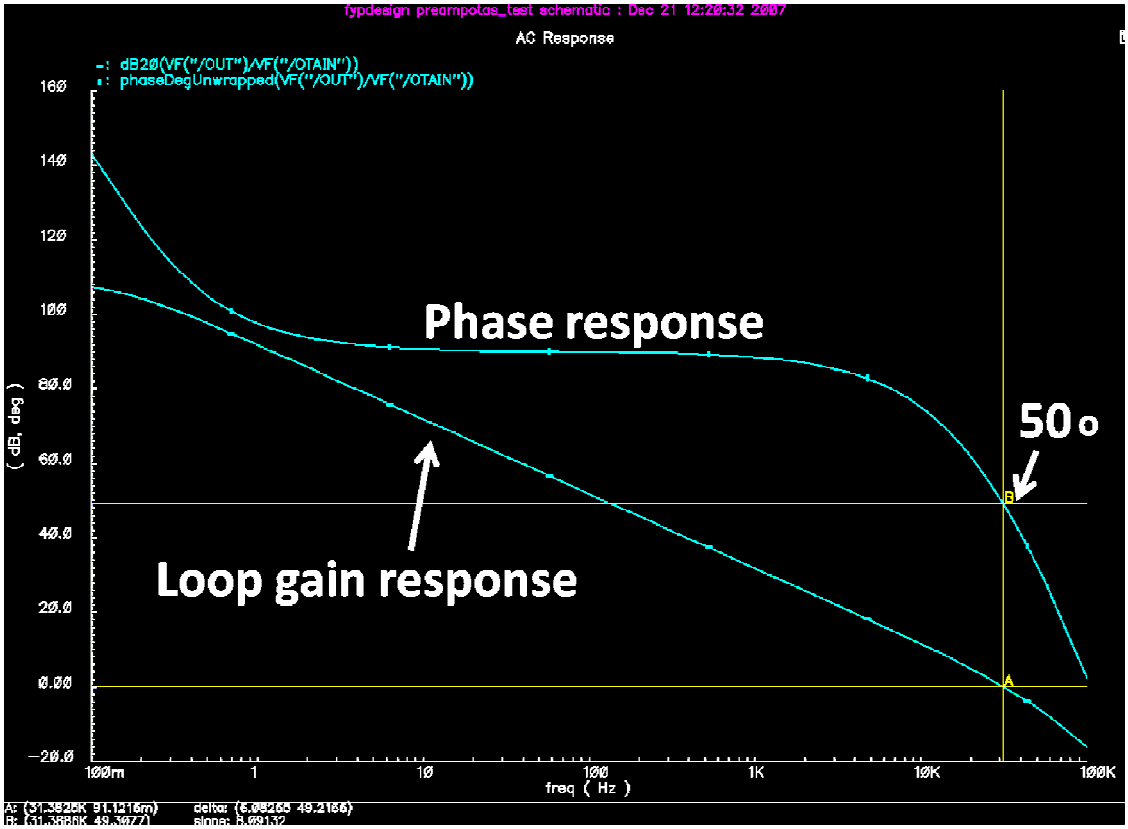


Figure 4.9 Phase response of LN-AMP.

As for the noise performance, the input referred noise spectral density and integrated noise is shown in Figure 4.10 and Figure 4.11 respectively. From Figure 4.10, the corner frequency of the input referred noise spectral density is about 5~6Hz. The input referred noise at 1Hz is at about $230\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ while the while noise level is about $100\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$.

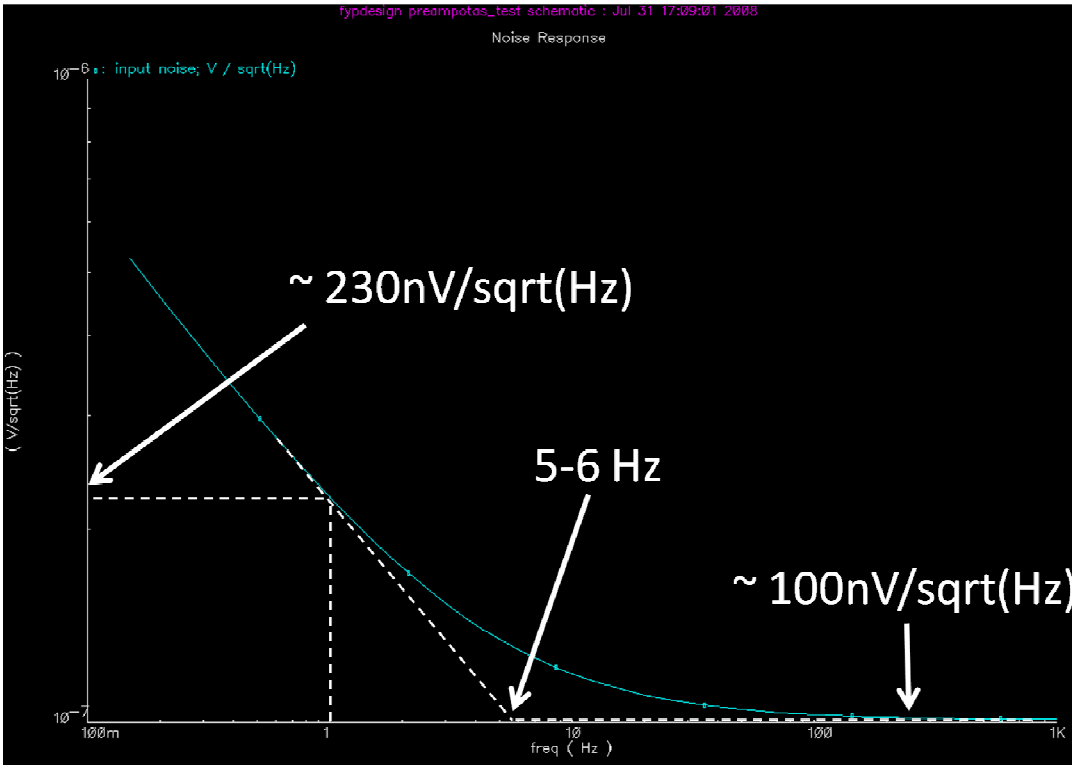


Figure 4.10 Input referred noise spectral density.

As for the integrated input referred noise, integrating the noise up to 150Hz, which is the ECG signal bandwidth, would give 1.3μV_{rms}. For the total in-band integrated input referred noise up to 192Hz, the noise spectral density within the bandwidth of the LN-AMP is integrated giving a value of 1.51μV_{rms} which is just meeting the specification.

As for the equivalent total input noise, the output referred noise is integrated up to $\pi/2$ of amplifier bandwidth which is about 300Hz, and then divided by the amplifier mid-band gain. The simulation result shown is about 1.7 μV_{rms}.

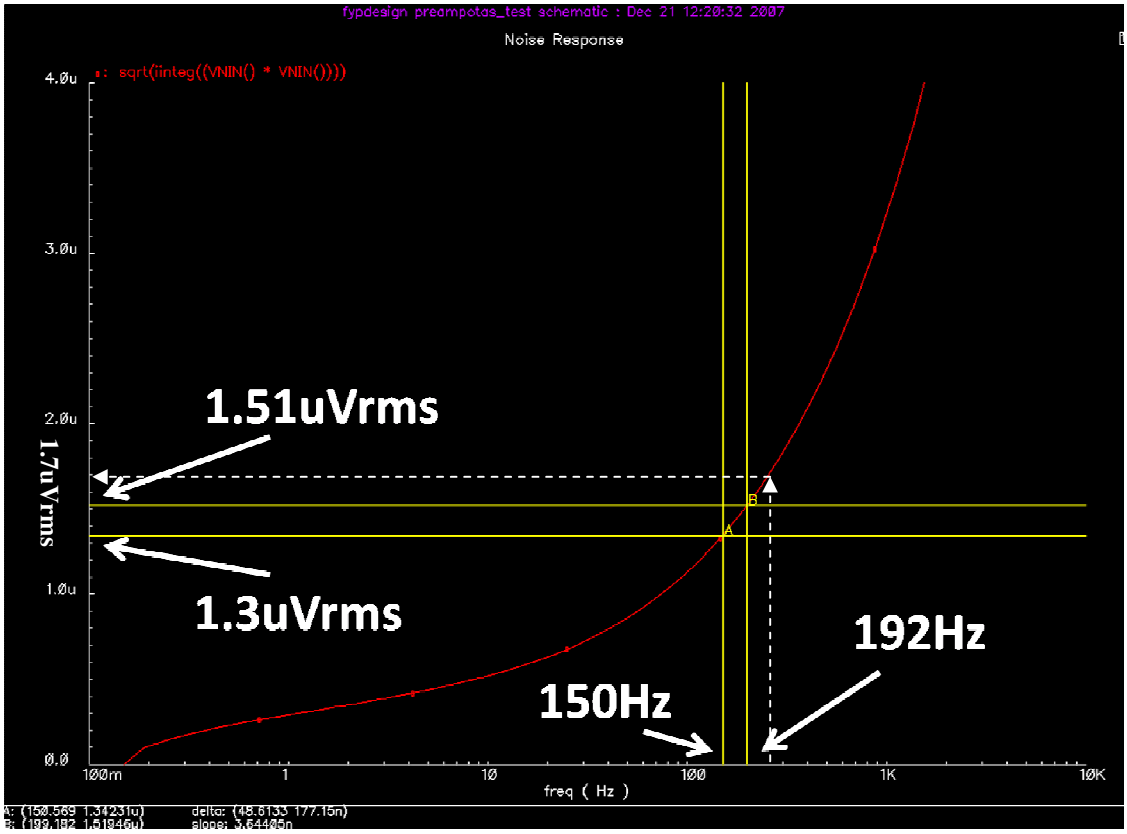


Figure 4.11 Integrated input referred noise.

The simulation results of the LN-AMP are summarized in Table 4.1.

Parameter	Value
Gain	200 V/V (46dB)
Bandwidth	0.13Hz to 192 Hz
Phase margin	50°
In-band integrated input referred noise[*1]	1.51 µVrms
NEF[*2]	5.21
Current consumption[*3]	2.2 µA

Table 4.1. Simulation results of LNA.

Notes: *1. Integrated input referred noise from 0.13Hz to 192Hz

*2. NEF refers to noise efficient factor with the following equation.

$$NEF = \overline{v_{ni,rms}} \cdot \sqrt{\frac{2I_{tot}}{\pi \cdot U_T \cdot 4kT \cdot BW}}$$

Where U_T is approximately 26mV.

*3. Total current consumption includes the biasing current.

4.2.2 SA-ADC Simulation Results

The frequency response of the comparator pre-amplifier is shown in Figure 4.12. Since an open loop approach is adapted, the pre-amplifier DC gain is as high as 70dB as shown in Figure 4.12. The unity gain frequency is around 1MHz giving about 70º phase margin. This would give enough headroom for stability concern when the pre-amplifier is closed-loop to undergo input offset cancellation operation.

Figure 4.13 shows the transient response of the overall comparator when the comparator is input with a 100μV signal at 32 kHz clock rate. The comparator is turned off during the sampling phase of A/D conversion and starts output during conversion phase.

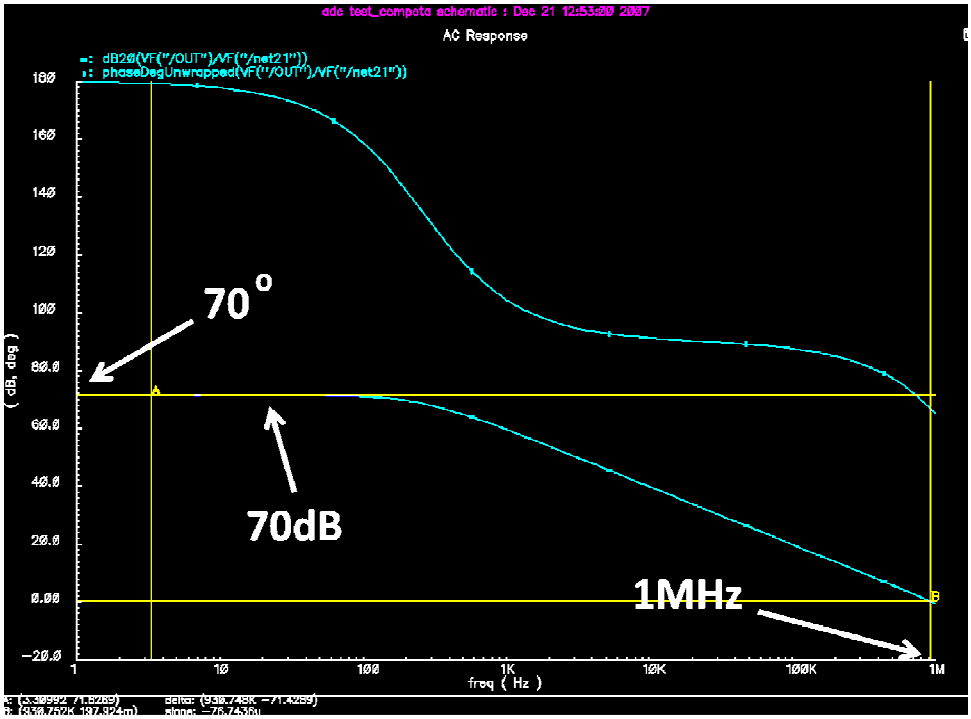


Figure 4.12 Frequency response of the comparator preamp.

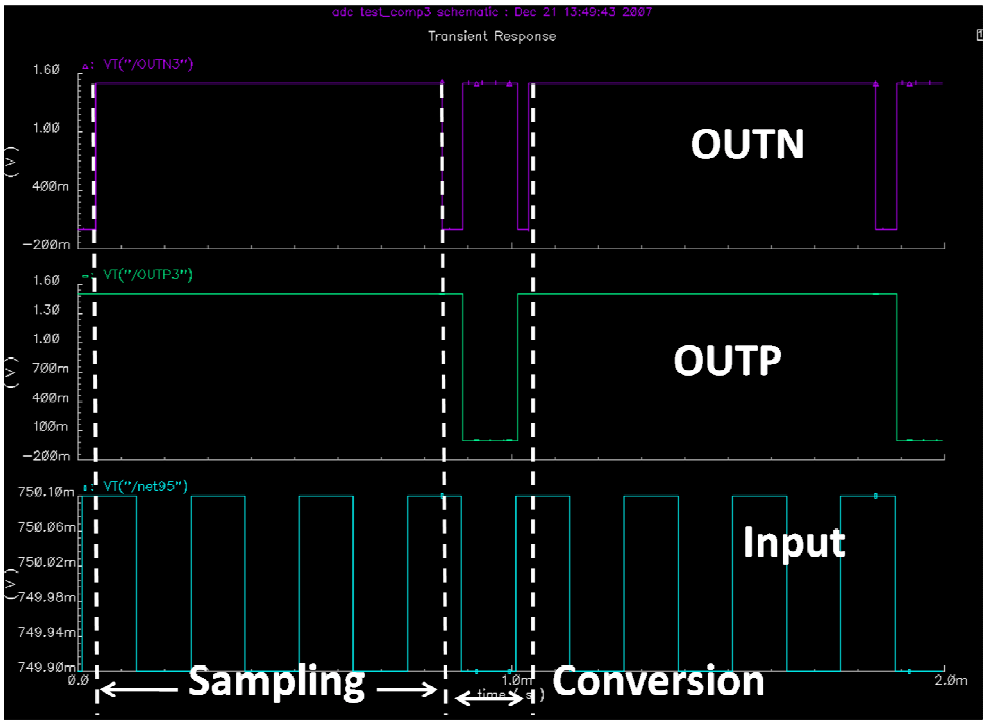


Figure 4.13 Transient results of overall comparator.

Figure 4.14 shows a complete sample-and-hold operation, together with the A/D conversion. The voltage at the input node of the ADC is sampled to the desired voltage level during sampling phase. Following that, the ADC conversion is completed during the hold phase. It can be seen that the voltage level at the ADC input node successively approximate to $V_{DD}/2$ to complete the A/D conversion.

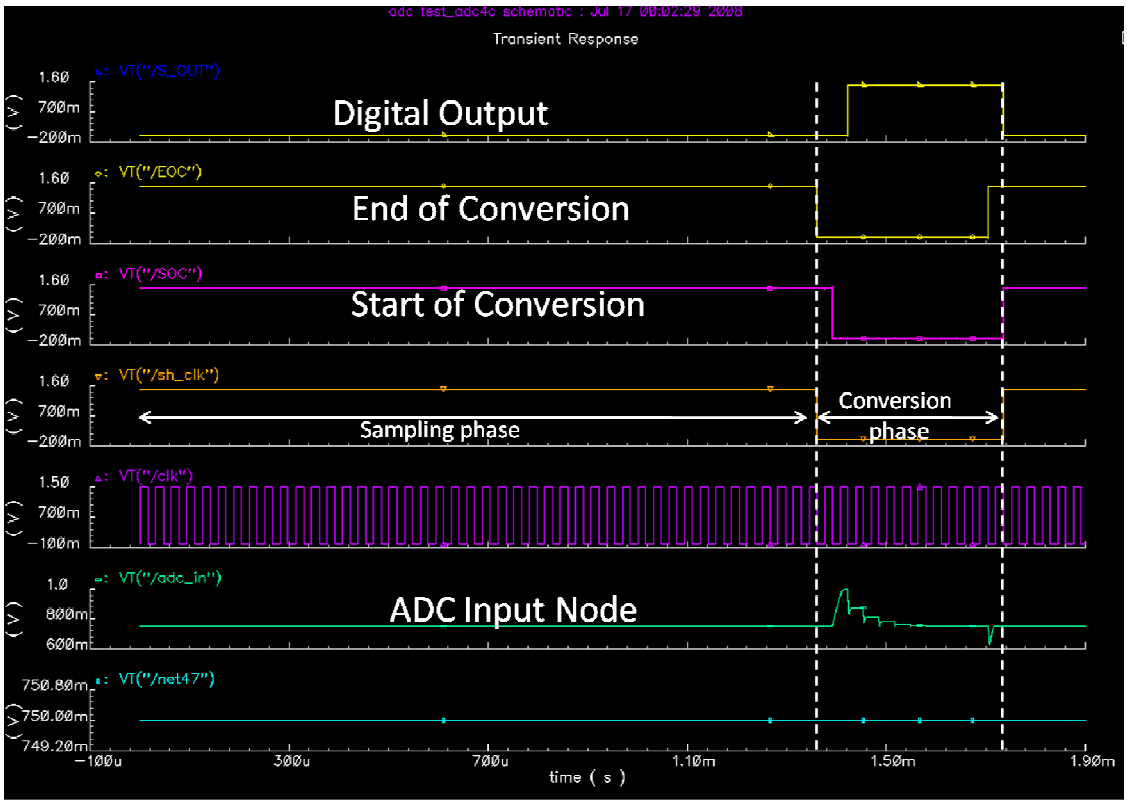


Figure 4.14 A complete sample-and-hold operation with the A/D conversion.

The simulation results of ADC are summarized in Table 4.2. Due to low clock rate and dynamic nature, the total current consumption is only 0.6μA with comparator consuming most of the current.

Parameter	Value
Comparator pre-amplifier gain	70dB
Comparator resolution	100 µV
ADC resolution	11 bit
ADC sampling rate	500 Hz
Comparator Current	0.5 µA
ADC current (excluding comparator)	0.1 µA

Table 4.2 ADC simulation results summary.

Parameter	Value
LN-AMP current	2.1 µA
Comparator current	0.5 µA
ADC current (digital)	0.1 µA
Bias current	0.1 µA
Total current	2.7 µA

Table 4.3 Overall power consumption distribution of each block.

CHAPTER 5 Measurements and Discussions

This chapter will discuss on the measurements results of the design. After chip fabrication, the packaged die was sent back from the foundry. A PCB was designed for chip measurement purpose. The PCB design is attached in Appendix B. In the latter section of this chapter, some discussions on the measurement results and issues encountered during testing will be elaborated.

The core chip area is 1.06mm^2 without pads, with dimension of 1000µm by 1060µm. A die photograph of the chip is shown in Figure 5.1.

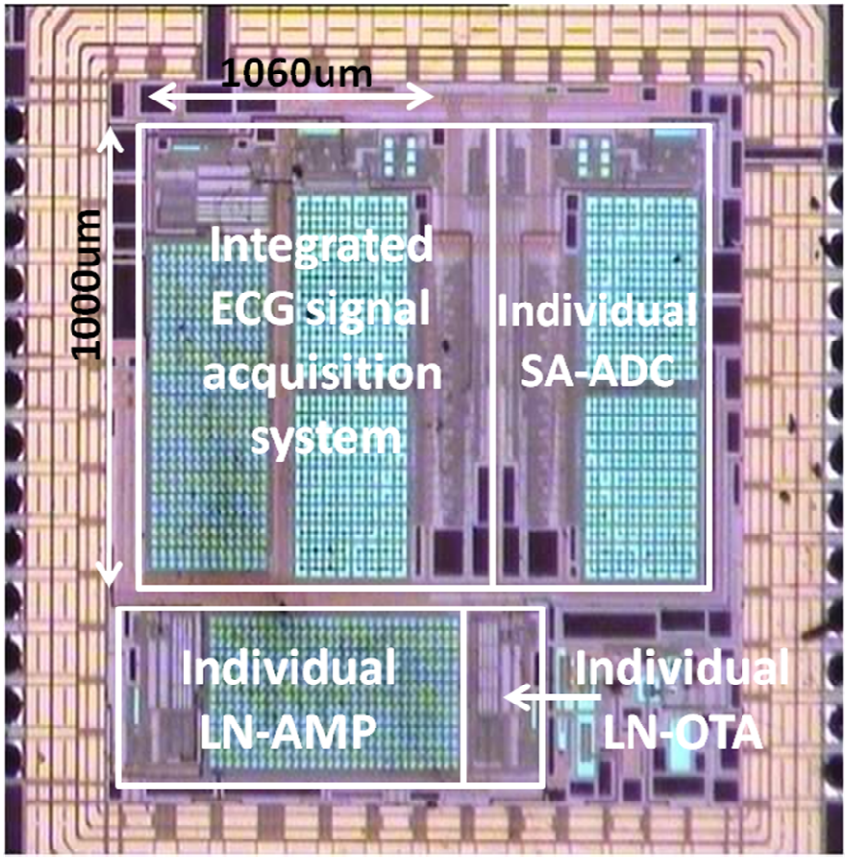


Figure 5.1 Die photograph.

5.1 Measurement Results

After receiving the fabricated chips, various testing and evaluations were performed on the design [34]. The measurement results can be separated into two parts. First part is the measurement result of individual blocks and next is the overall measurement result.

5.1.1 LN-AMP Measurement Results

An individual LN-AMP circuit was fabricated together with integrated system to ease the difficulty of extracting LN-AMP performance from overall system. The individual block is loaded with 128pF, approximately the same with the capacitive load in the integrated system. This would provide a good estimation for the LN-AMP performance.

For LN-AMP measurements, basically the testing covers the LN-AMP performance on differential mode gain, bandwidth, input referred noise, total harmonic distortion (THD), common mode rejection ratio (CMRR), and power supply rejection ratio (PSRR). Test setups and the corresponding results are discussed in the following.

5.1.1.1 Differential Mode Gain and Bandwidth

For differential mode gain evaluation, the input of the LN-AMP is connected to a differential sinusoidal waveform with $1mV_{PP}$ amplitude and 10Hz frequency. The output of the LN-AMP is observed using an oscilloscope to check the waveform and output FFT plots. The test setup is as shown in Figure 5.2.

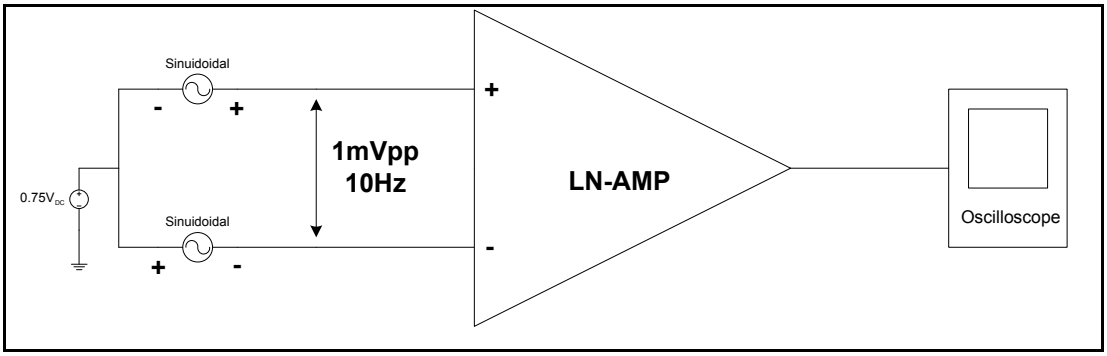


Figure 5.2 Test setup for differential mode gain measurement.

From test setup in Figure 5.2, the measured gain is 200V/V which is equivalent to 46dB. The measured gain was double-confirmed by varying the input amplitude from 1mV$_{PP}$ to 3mV$_{PP}$. Rough estimation for bandwidth is about from below 10mHz to about 190Hz. This is confirmed by frequency response extracted from the test setup in Figure 5.3.

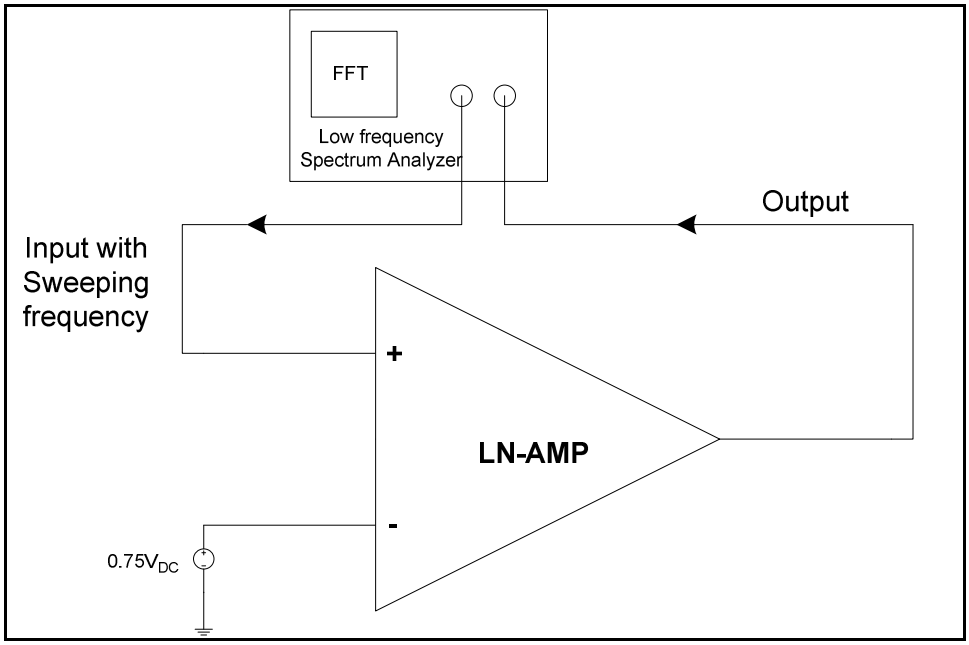


Figure 5.3 Test setup for frequency response measurement.

Using test setup in Figure 5.3, the LN-AMP input is fed in an input with sweeping frequency from the low frequency dynamic spectrum analyzer. The output of the LN-AMP is connected back to the spectrum analyzer where the testing instrument will calculate the gain and phase response of the LN-AMP at the input frequency. By sweeping the input frequency, the spectrum analyzer will automatically calculate and plot the magnitude and phase response.

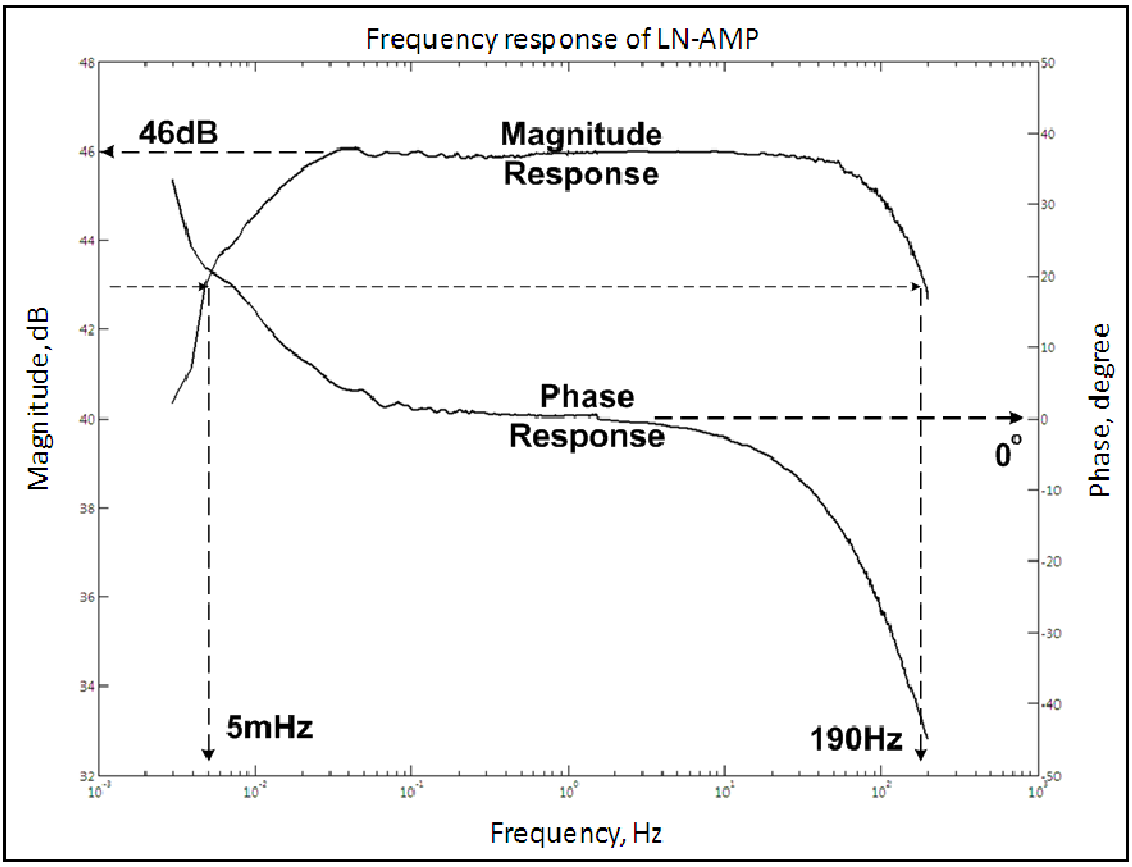


Figure 5.4 Frequency response of the LN-AMP.

Figure 5.4 shows the frequency response of the LN-AMP extracted from the low frequency spectrum analyzer, which includes both magnitude response and phase response. The mid-band gain is 46dB while the bandwidth covers from 5mHz to 190Hz.

Basically the gain and low pass 3dB cut-off frequency are meeting both simulation results and specifications. As for the high pass 3dB cut-off frequency, it is much lower than the simulation results though it is meeting the specifications. This will be further discussed later in section 5.2.

5.1.1.2 Input referred noise

The input referred noise is measured using the test setup in Figure 5.5.

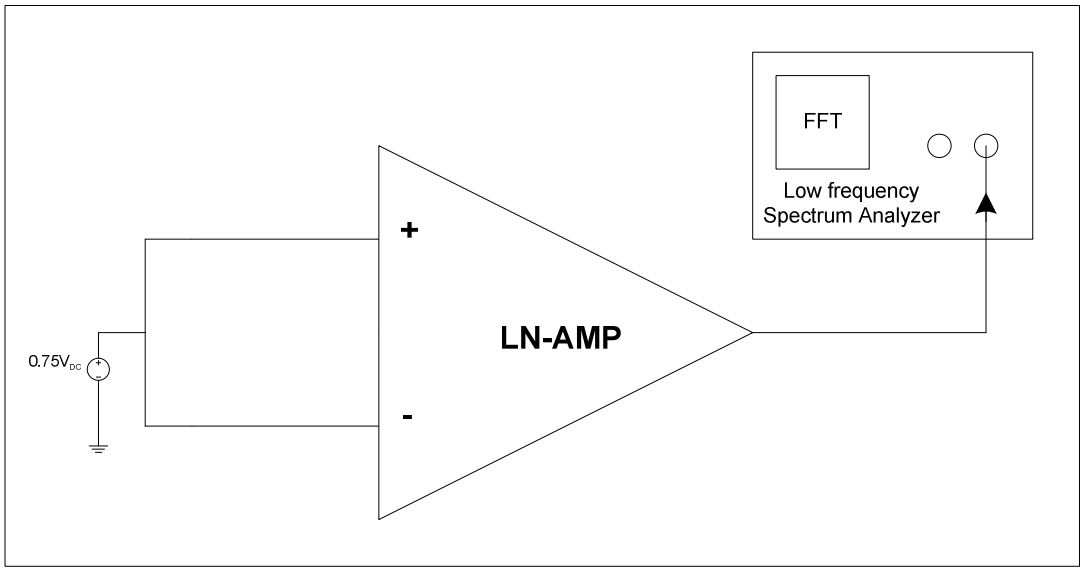


Figure 5.5 Test setup for input referred noise measurement.

As shown in Figure 5.5, both input of the LN-AMP are connected together to a clean DC source of $0.75V_{DC}$, equivalent to $V_{DD}/2$. The output of the LN-AMP is connected to the low frequency dynamic spectrum analyzer to record the output noise. Following this, the equivalent input referred noise is calculated using the output noise recorded divided by the magnitude response acquired earlier on. The input referred noise obtained is plotted in Figure 5.6.

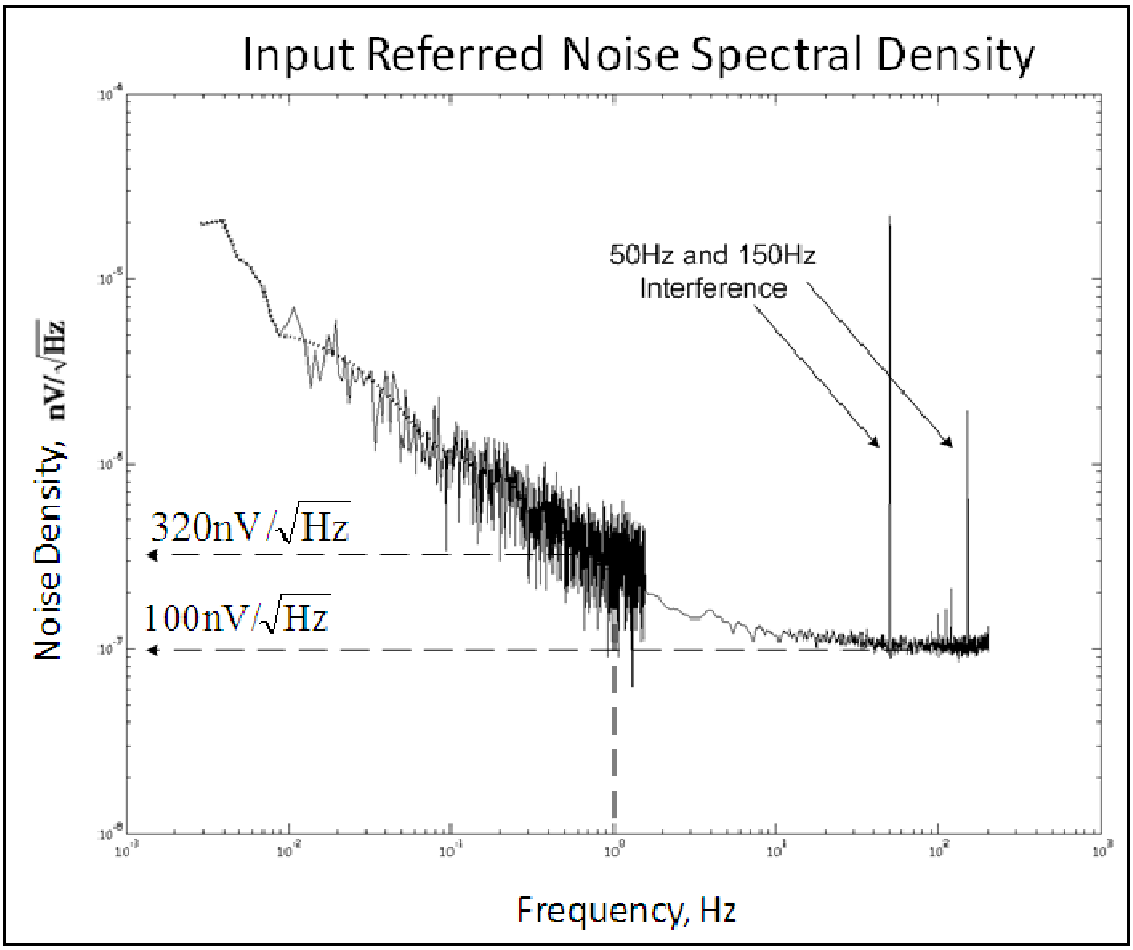


Figure 5.6 Input referred noise of the LN-AMP.

From Figure 5.6 it can be seen there is 50Hz and 150Hz interference from the power line. The white noise level is about $100\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$, close to simulation results. However, the flicker noise level is higher than expected. The noise level at 1Hz is about $230\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ in simulation while measurement results gives $320\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. The noise corner frequency is also higher due to the fact of higher flicker noise level in physical measurement. Measurement results is about 10~20Hz while in simulation it is only about 5~6Hz.

In Figure 5.6, the low frequency noise spectral density up to 1.5Hz can be seen fluctuating a lot. This is due to the insufficient averaging of data where extremely long testing period is needed for ultra low frequency range. Hence some post-processing was done to average out the low frequency range noise spectral density. The post-processed input referred noise up to 1.5Hz is plot in dotted line in Figure 5.6.

As for the integrated input referred noise, output referred noise is integrated to equivalent bandwidth, which is equivalent to $\pi/2$ of amplifier bandwidth, and divided by the amplifier mid-band gain to give equivalent input referred noise. The output referred noise is shown in Figure 5.7.

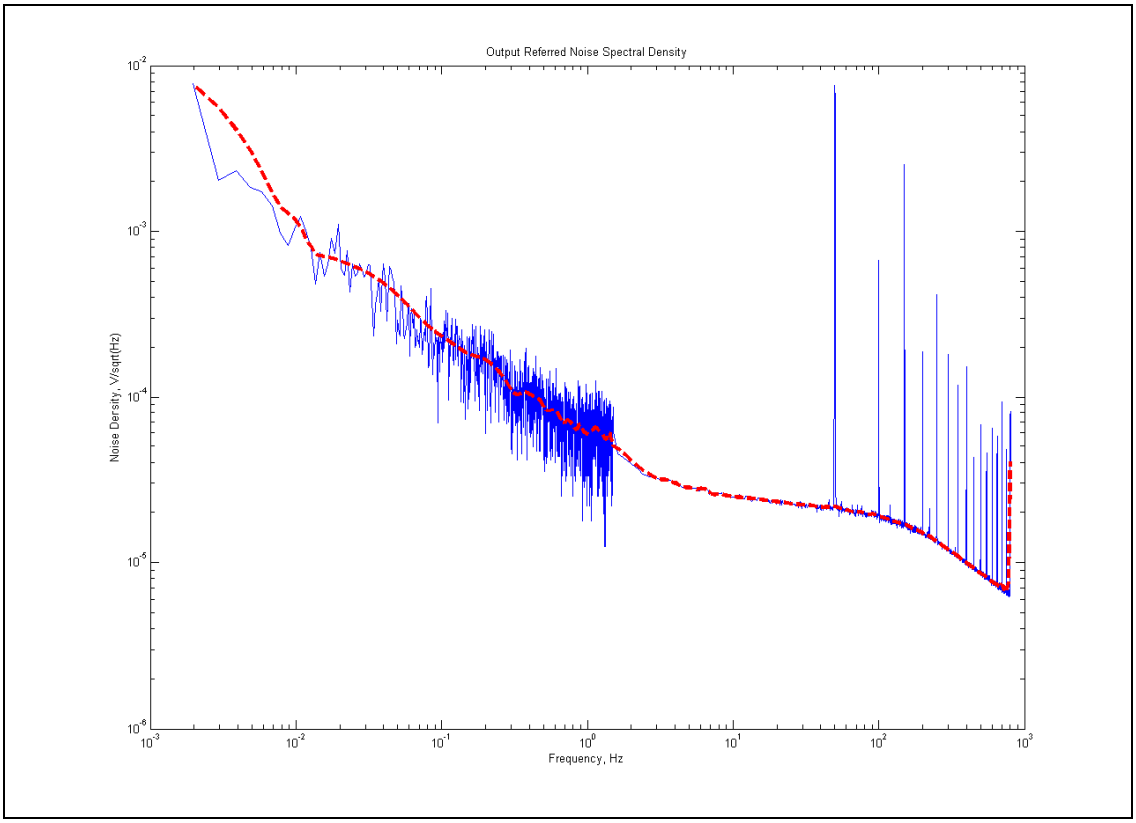


Figure 5.7 Output referred noise of the LN-AMP.

The dotted line is the averaged out output referred noise and is integrated up to 300Hz to give an equivalent total output integrated noise. The total input referred integrated noise is obtained by dividing the equivalent total output integrated noise by mid-band gain, which is about 199.5. The result is about 1.862 μV_{rms}, which is higher than 1.7μV_{rms} in simulation. Further discussion will be elaborated in the section 5.2.

5.1.1.3 Common mode rejection ratio

The test setup for common mode gain measurement is shown in Figure 5.8.

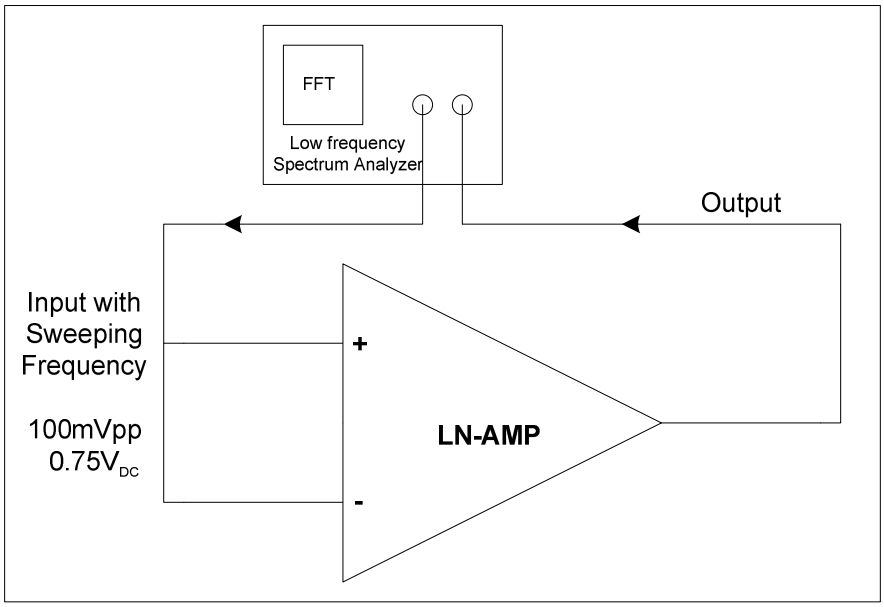


Figure 5.8 Test setup for common mode gain measurement.

Using test setup shown in Figure 5.8, both inputs of the LN-AMP are connected together to an input with sweeping frequency from the low frequency dynamic spectrum analyzer. The input level is set to $100mV_{PP}$ with 0.75V DC biasing. The output of the LN-AMP is connected back to the spectrum analyzer to obtain the output FFT plot and hence the common mode gain. By sweeping the input frequency, the spectrum analyzer will automatically calculate the magnitude response over a frequency range.

From measurement results, the common mode gain is about -22.8dB covering from 1Hz to 200Hz. The common mode rejection ratio is given by the following equation (5.1).

$$\text{CMRR} = 20 \lg\left(\frac{A_{DM}}{A_{CM}}\right) \qquad (5.1)$$

A_{DM} is the differential gain and A_{CM} is the common mode gain.

By calculate using equation (5.1), the common mode rejection ratio is about 68.8dB in frequency range of 1Hz to 200Hz. The plot is shown in Figure 5.9.

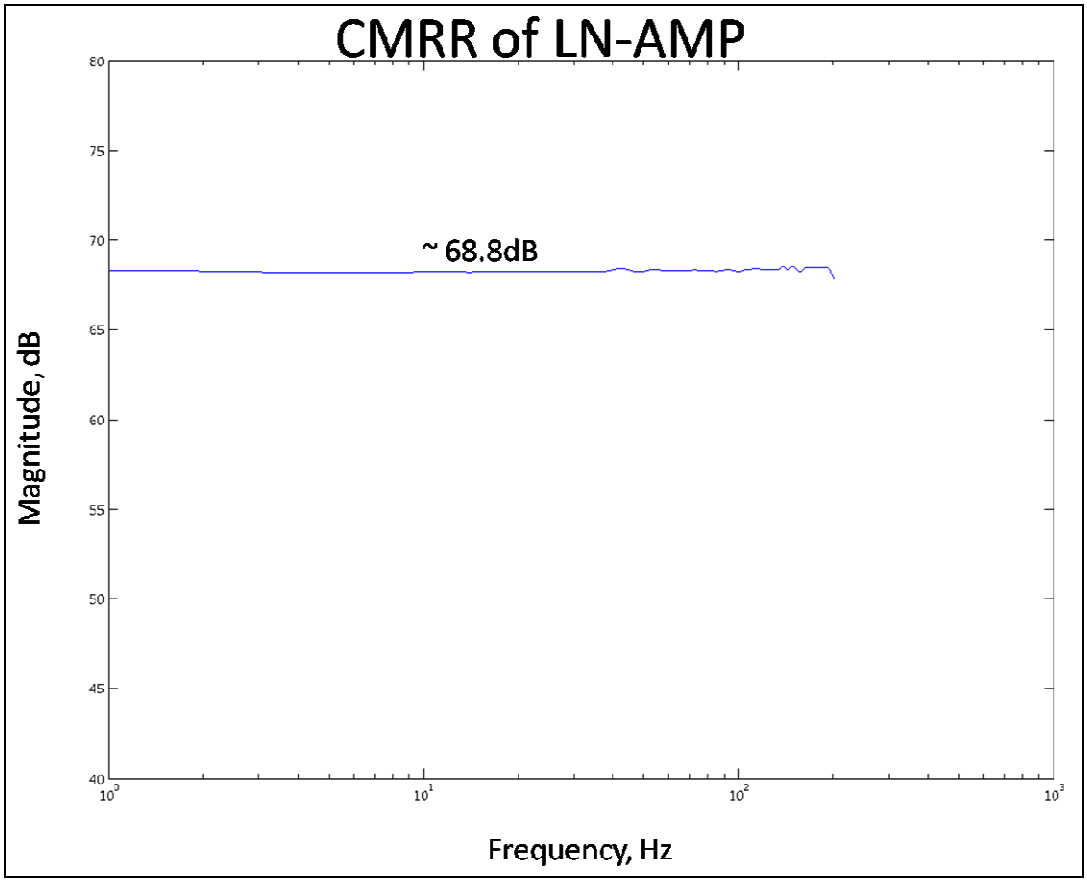


Figure 5.9 Measured CMRR Plot.

5.1.1.4 Power supply rejection ratio

The test setup to measure positive power supply rejection ratio is shown in Figure 5.10. The inputs of the LN-AMP are biased to $0.75V_{DC}$ equivalent to $V_{DD}/2$ while the testing input source from the spectrum analyzer is connected to V_{DD} power supply of LN-AMP. The output is connected back to spectrum analyzer to obtain the gain from V_{DD} power supply to the LN-AMP output.

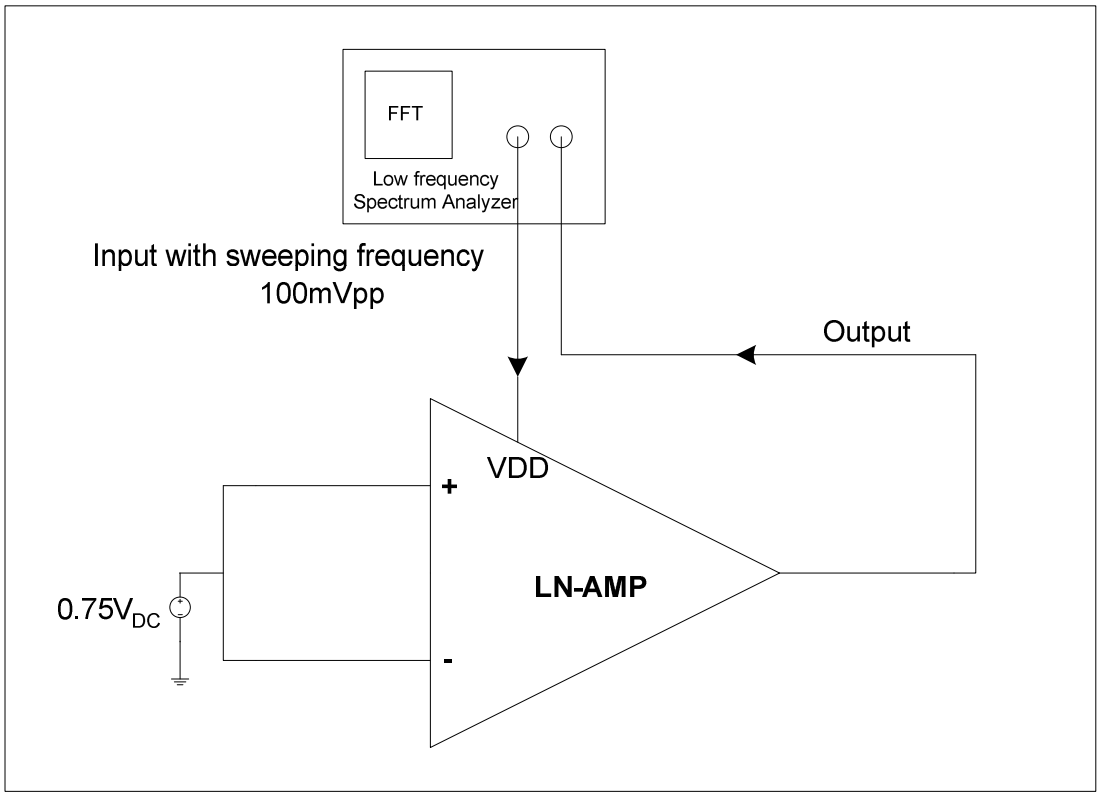


Figure 5.10 Test setup for positive power supply rejection ratio measurement.

Power supply rejection ratio (PSRR) of an amplifier is defined as the gain from the input to the output divided by the gain from the supply to the output [17]. As the voltage can be supplied from V_{DD} or V_{SS} (ground), there are positive and negative power supply rejection ratio corresponding to interference through V_{DD} or ground. The positive power supply rejection ratio with reference to interference through V_{DD} is measured here. From the measurement results, the positive PSRR is about 59.2dB from 1Hz to 200Hz. The PSRR plot is shown in Figure 5.11.

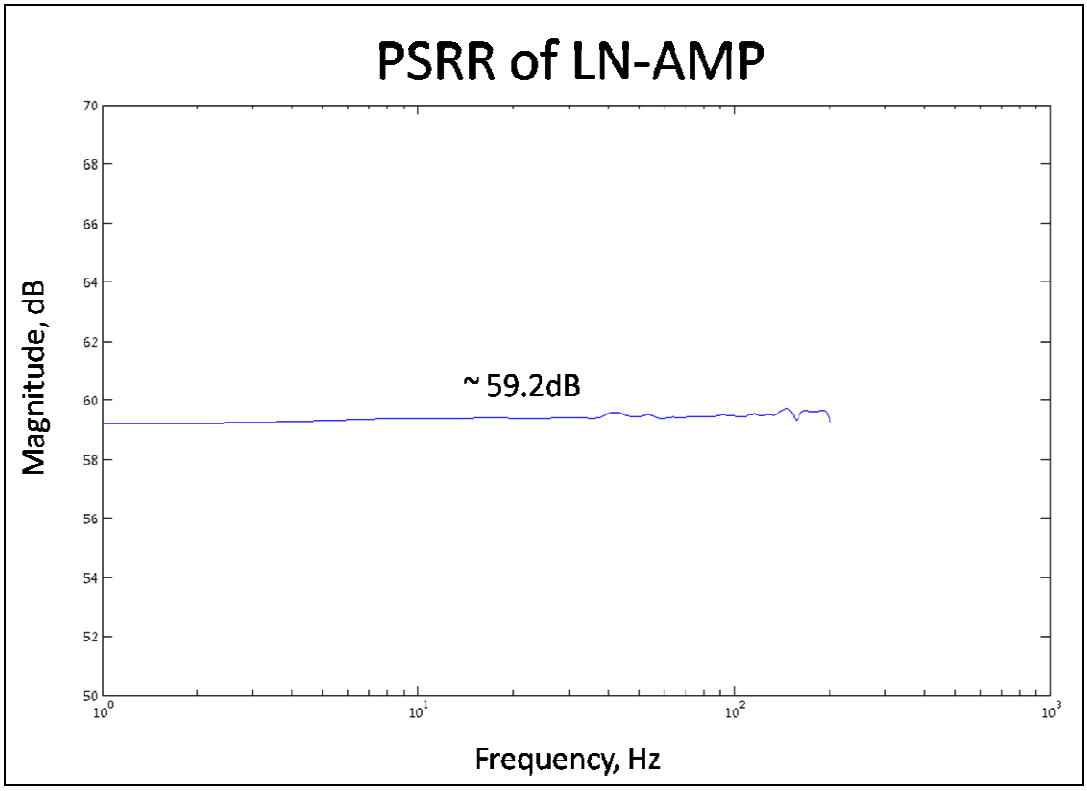


Figure 5.11 Measured CMRR Plot.

5.1.1.5 Summary

The overall measurement results of the LN-AMP are summarized in the following table. The current consumption which includes the biasing current is measured to be around 2.2μA, meeting the simulation results.

Parameters	Values
Supply voltage	1.5V
Amplifier gain	46dB
Amplifier 3dB bandwidth	5mHz – 190Hz
Amplifier in-band input referred noise	$1.862\mu V_{rms}$
Amplifier CMRR	68.8B
Amplifier PSRR	59.2dB
Current consumption	2.2μA

Table 5.1 Summary of overall measurement results of LN-AMP.

5.1.2 SA-ADC and Overall Measurement Results

The test setup to evaluate overall system performance is shown in Figure 5.12. The inputs of the integrated system are basically the inputs of the LN-AMP. In this test setup, the inputs are connected to source generator to feed in different signals, including sinusoidal and ramp waveform, to evaluate the performance. The outputs of the Device-Under-Test (DUT) are primarily the ADC serial output, start of conversion (SOC) signal, and end of conversion (EOC) signal. The outputs are connected the Agilent 1672G Logic Analyzer to obtain the needed results.

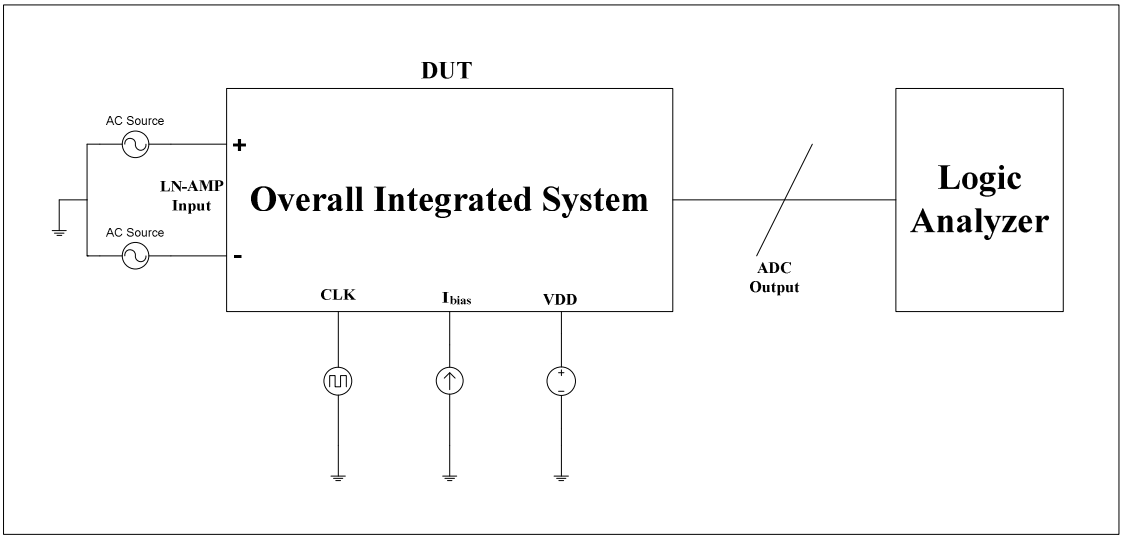


Figure 5.12 Test setup for overall system performance measurement.

The above test setup was used to measure the Effective Number of Bit (ENOB) of the ADC. ENOB is basically an effective and more accurate reflection of the accuracy of the ADC. The ENOB performance of an ADC can be found through the Signal-to-Noise Ratio (SNR) of the ADC digital output. ENOB of an ADC is related to SNR through

$$SNR = 6.02N + 1.76 \quad (5.2)$$

where SNR is in terms of dB and N reflects number of bit for the ADC. Due to the ADC output is digital in nature, Signal-to-Quantization-Noise Ratio (SQNR) is used instead of SNR.

However, due to some difficulties in test setup of the stand-alone ADC which will be discussed further in section 5.2, the test setup for overall system measurement in Figure 5.12 is used to measure the SQNR. Hence, the SQNR measured includes the effect from the input stage LN-AMP.

The input signal used is a 1Hz frequency 3.5mV_{PP} differential sinusoidal waveform. Clock frequency is set to 30 kHz to achieve a sampling rate of 500S/s. The output is acquired through the logic analyzer and converted back to digital code using Matlab program. By using Matlab program also, the digital output code is transformed into power spectrum density plot, as illustrated in Figure 5.13.

In computing SQNR, all external interference components and all harmonic components of the signal are to be excluded. From Figure 5.13, the overall system achieves a SQNR of 57.7dB. Using equation (5.2), it yields an ENOB of 9.3 bit.

To complete the overall testing, the overall integrated system was used to record a signal from an ECG signal simulator (model ST-16 from ST-Electromedicina). The digital output code is shown in Figure 5.14. Small glitches are observed due to the 50Hz power line interference.

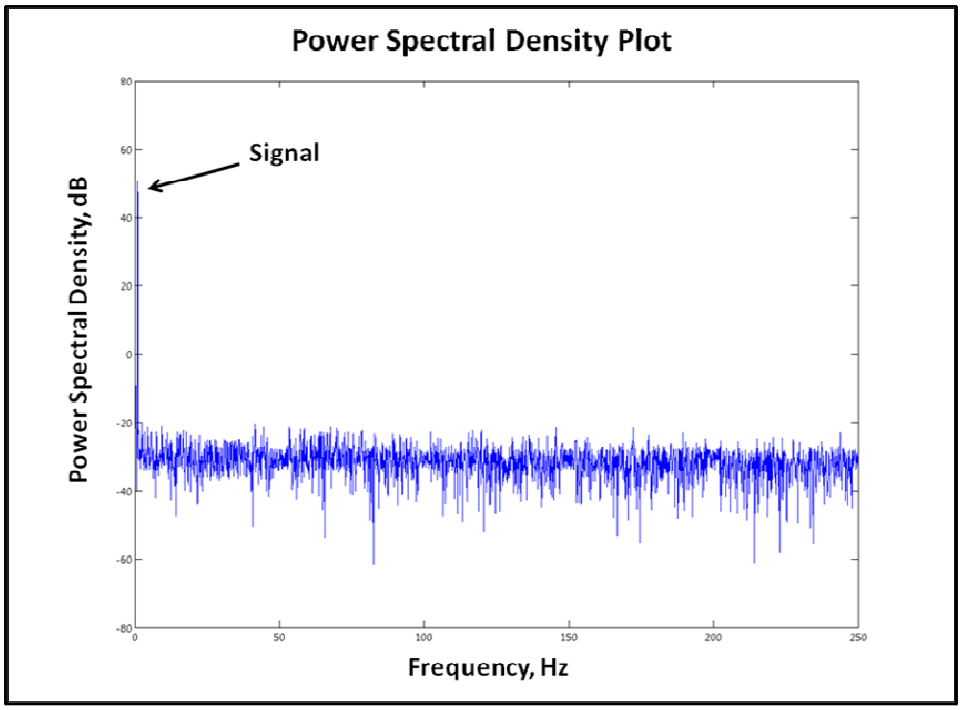


Figure 5.13 Power spectrum density plot of overall system output.

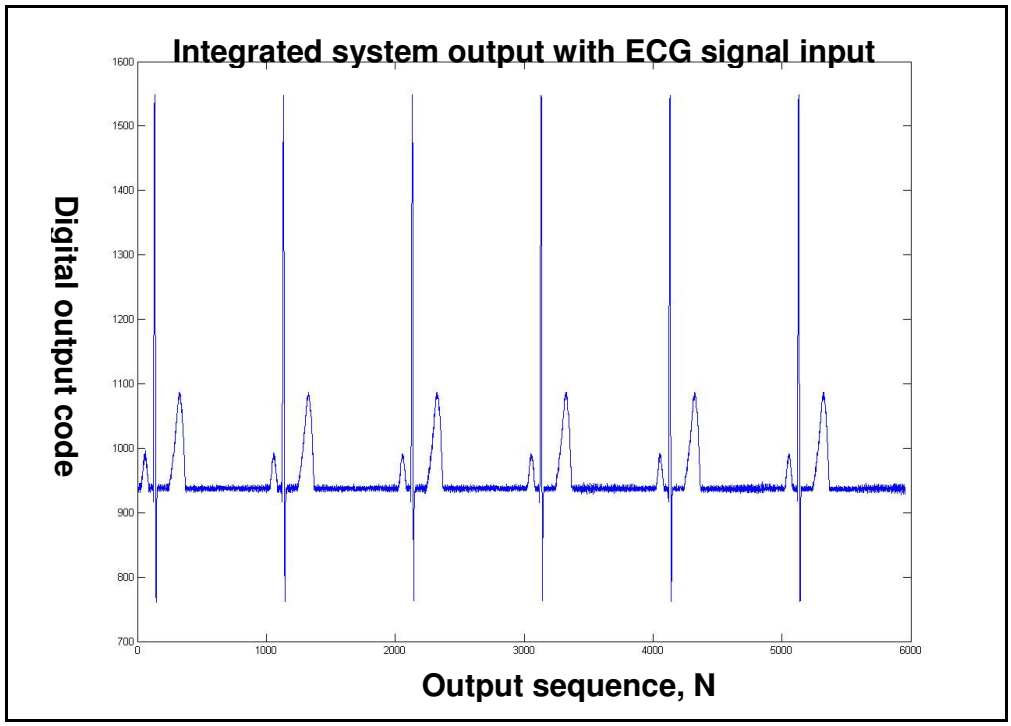


Figure 5.14 Integrated system output with ECG signal input.

Finally, overall measurement results of the overall integrated system are summarized in Table 5.2.

Parameters	Values
Supply voltage	1.5V
ADC sampling rate	500S/s
ADC ENOB	9.3 bit
Total current	2.7μA
Core chip area	1.06mm^2

Table 5.2 Summary of overall measurement results for integrated system.

5.2 Testing Issues and Discussions

In the process of measuring the performance of the chip, there are several main testing issues encountered and will be discussed in this section.

5.2.1 LN-AMP Input referred noise

The measured integrated input referred noise is found to be higher than the expected value obtained from simulation. In simulation results shown in chapter 4, the in-band integrated input referred noise is 1.7μV$_{rms}$. However, as depicted in the previous section, the measured value is 1.862μV$_{rms}$, about 0.162μV$_{rms}$ higher than the simulation results.

There are two factors that results in higher input referred noise. First factor is regarding to the bandwidth of the LN-AMP. The in-band integrated input referred noise

integrates the input referred noise spectral density within the bandwidth of the LN-AMP. The measured low pass 3dB cut-off frequency at 190 Hz is nearly the same with simulation results at 192Hz. However, the measured high pass 3dB cut off frequency is much lower than the simulation results. In simulation, the cut-off frequency is about 130mHz while measured result is about 5mHz which is more than a decade away. The higher bandwidth results in more noise to be integrated for the in-band input referred noise parameter.

Second factor is the higher level of flicker noise in measurement than simulation. From Figure 5.6 it can be seen that the flat thermal noise level is about $100\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ near to simulation results. However, the flicker noise level at 1Hz is recorded to be $320\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ as compared to $230\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ in simulation. Furthermore the difference at lower frequency is even greater. At 200mHz, simulation result shows $430\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ while measurement reveals an almost double value of $800\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$.

This clearly shows the simulation model underestimates the flicker noise level in physical device. Hence in future design, an overestimation on noise level is definitely needed if the same simulation model is to be used.

5.2.2 ADC parameters measurement

In the ADC measurement test setup, a stand-alone ADC in the fabricated chip was initially used as the DUT. However, the S/H circuit is inevitable in measuring the performance of an ADC. Due to inexperience in ADC measurement and time-constraint, an internal S/H circuit was not integrated with the individual ADC block.

To solve this problem, an external switch was used to form the S/H circuit with the on-chip DAC capacitor array in the individual ADC. For such a simple S/H circuit, the time constant, τ is given by

$$\tau = R_{ON}C_H \tag{5.3}$$

where R_{ON} is the on-resistance of the switch and C_H is the holding capacitor. The value of τ would decide the maximum holding time for an S/H circuit. In this case, C_H is approximately 128pF represented by the on-chip DAC capacitor array.

However, measurement revealed that the voltage at the ADC input node cannot be held throughout the whole conversion phase. While R_{ON} of the external switch is at very low level, the time constant cannot be improve since C_H is fixed. Under such circumstances, the performance of the ADC can only be extracted from full integrated system measurements.

In integrated system architecture, the input stage is a LN-AMP followed by the SA-ADC. Hence the full integrated system measurements cannot fully reflect the performance of the individual ADC as the input stage LN-AMP has introduced non-ideality to the signal before ADC. This is reflected from the power spectral density plot of the ADC digital output in Figure 5.10. The harmonics are basically introduced by the LN-AMP while the noise floor is elevated by the device noise from LN-AMP. These would deteriorate the SQNR and hence the ENOB measured.

Besides that, the DNL and INL performance are seriously affected due to the same reason. A ramp input signal is used in the test setup shown in Figure 5.11 for DNL and INL measurement. However, there are constraints on the input where the frequency and magnitude of the ramp input signal is restricted by the LN-AMP. Using a $6mV_{pp}$ 50mHz

ramp input signal, the DNL reaches 4LSBs. In overall, these results cannot fully reflect the actual performance of the ADC due to the mentioned factors.

5.2.3 External interference

Another issue observed during measurement is the external interference on the measurement results, especially the 50Hz power line interference. The effect can be seen obviously in the input referred noise and ADC output power spectral density plot.

To minimize this interference, a notch filter at 50Hz can be used in the system. However, very large capacitor and very low transconductance are needed to realize a high order filter with notching at frequency as low as 50Hz. There is a limitation on area used if to achieve a fully integrated portable device while additional block would add to power consumption as well. Hence it is hardly advisable to add a notch filter in the system.

A workable solution is to process the digital output using digital filter at base station. As to be discussed in chapter 6, if future work is done to transmit the digital signal output wirelessly to a base station, it will be more sensible to filter the 50Hz interference at the base station.

CHAPTER 6 Conclusion and Future Work

6.1 Conclusion

The design an ECG signal acquisition chip was presented in this thesis. The design consists of a Low Noise Amplifier (LN-AMP) and an 11 bit Successive Approximation Analog-to-Digital Converter (SA-ADC). Overall work done for this research included circuit design, layout implementation, post-layout verification, testing setup and chip measurements.

With careful optimization of transistor sizes and operation in weak inversion region for better g_m/I_D efficiency, the chip achieves a performance of $1.862\mu V_{RMS}$ input referred noise over the system bandwidth from 5mHz to 190Hz. The sampling rate of the system is set to 500S/s with a 30 kHz clock rate. Overall system achieves an Effective Number of Bit (ENOB) of 9.3 bit with a measured SQNR of 57.7dB. The integrated system consumes a total current of 2.7μA under 1.5V supply voltage, which gives a power consumption of 4.05μW. A comparison with other works is presented in Table 6.1.

Design	[8] *1	[12] *2	[13] *3	This work
Process	0.5µm CMOS	1.5µm CMOS	0.35µm CMOS	0.35µm CMOS
Supply voltage (V)	+/- 1.5	+/- 2.5	1	1.5
Mid-band Gain (dB)	0 - 80	39.5	40.2	46
Bandwidth (Hz)	0.3 – 150	25m – 7.2k	3m – 245	5m – 190
Input referred noise (µVrms)	0.86	2.2	2.7	1.862
Current consumption (µA)	485	16	2.3	2.7

Table 6.1 Comparison between few reported ECG chips and this work.

Notes: *1. Chip includes multiplexer, rail-to-rail IA, programmable gain amplifier, low pass filter, output scaling amplifier and digital control, for EEG and ECG signal acquisition.

*2. Chip includes a LN-AMP for general purpose.

*3. Chip includes a LN-AMP and a SA-ADC for ECG signal acquisition.

6.2 Future Work

As compared in table 6.1, noise efficient factor of the present LN-AMP design is considerably less than works in [12] and [13] although input referred noise is lower with comparable total system power consumption. The noise efficient factor reflects the trade-

off between input referred noise performance and current consumption. More works could be done to improve on the transconductance of the LN-OTA to achieve a better current efficiency with present input referred noise level.

As for the ADC, more efforts are needed to improve the SQNR performance. In addition, there are issues in the ADC test setup as mentioned in chapter 5. Hence in future work more attentions are required on the test plan in order to avoid such an issue happening once more.

Another possible future improvement is on the portability of the system. It would be a possible innovation to integrate a wireless transmission circuit to transmit the acquire data to a base station for post processing. As most of the post processing is in digital domain, letting the digital processing to be done at base station will greatly reduce the complexity of a signal acquisition chip and hence the power consumption. This would certainly enhance the battery life of a portable device.

In conclusion, a full integration ECG signal acquisition chip would be an ideal portable device for the use of non-invasive diagnostic measure and long-term recording. The research window is still open for further enhancing the performance.

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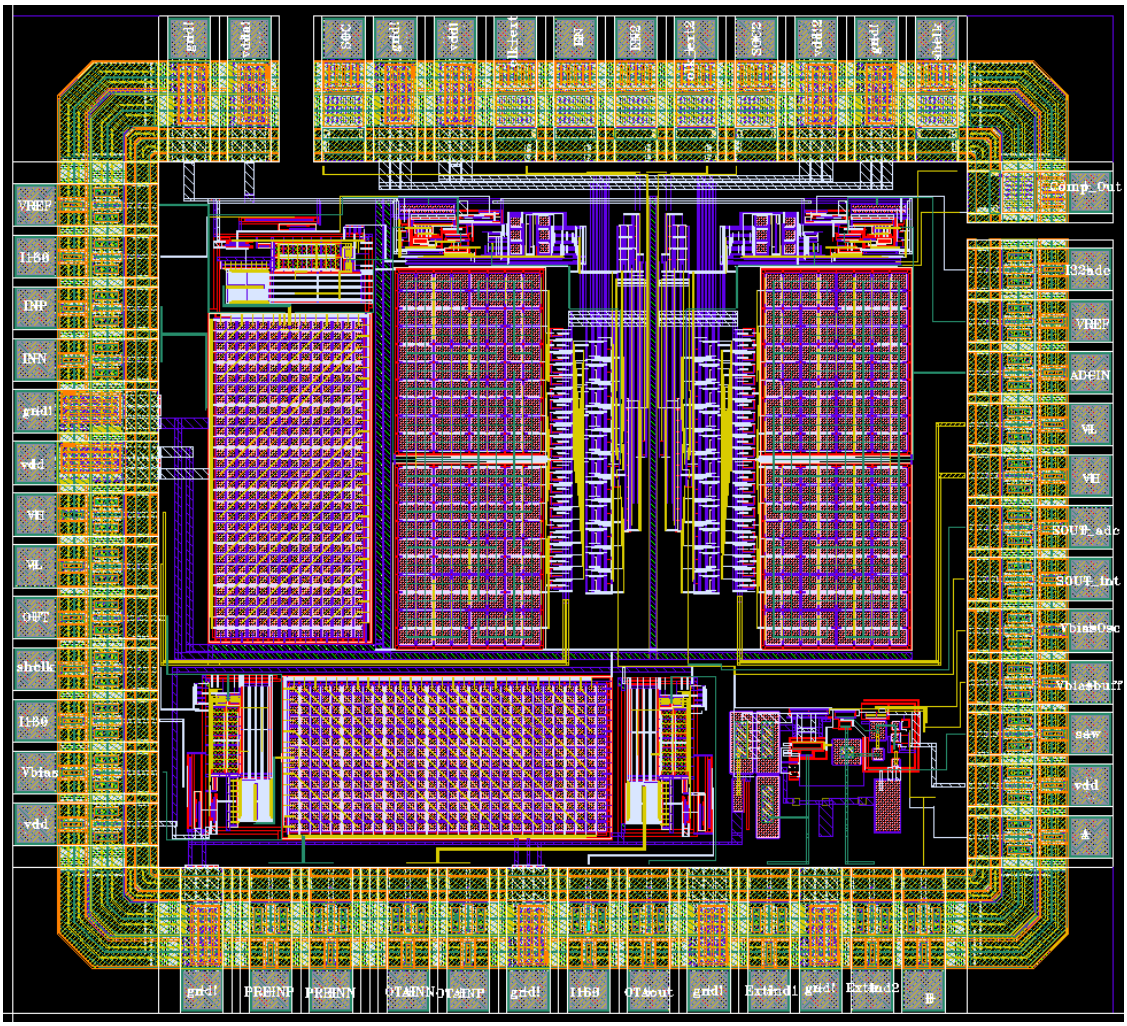
Appendix A

Overall chip layout with pads



Appendix B

PCB for chip measurement